SAVONIA

Update for X-Ray Beam Profile Monitor Motherboard and Firmware

Janne Himanen

Bachelor's Thesis

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Bachelor's degree (UAS)

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Tiivistelmä

Koulutusala Tekniikan ja liikenteen ala			
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Ohjaaja(t) yliopettaja Ari Suopelto, Savonia-ammattikorkeakoulu tohtori Gary Varner, University of Hawaii at Manoa			
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Tiivistelmä

Tämän opinnäytetyön tarkoituksena oli päivittää röntgensäteilynkuvantamislaitteen emolevy, firmware sekä tehdä tarvittavat testaukset. Työ tehtiin Havaijin Manoan yliopiston tuotekehityslaboratoriolle. Laite sijoitetaan valmistuttuaan Japanin Tsukubaan KEK:n (The High Energy Accelerator Research Organization) laboratoriossa sijaitsevaan Belle II -detektoriin. Tämä on osa SuperKEKB-hiukkaskiihdyttimen päivitystä, joka tuo KEK:n kiihdyttimelle maailman suurimman luminositeetin (8×10^{35} $cm^{-2}s^{-1}$).

Kuvantamislaitteeseen kuuluu emolevy, 128 vahvistinkorttia, kahdeksan tytärkorttia sekä firmware-alusta datan siirtoa varten. Emolevyn tarvitsemat päivitykset tehtiin PADS-piirilevyn suunnittelu ohjelmistolla. Vahvistimien testaukset suoritettiin käyttämällä verkkopiirianalysaattoria sekä oskilloskooppia. Olemassa oleva firmware ei ollut täysin toimiva, ja firmware-alustan vaihdon seurauksena vaihtui myös alustan FPGA-piiri (ohjelmoitava digitaalinen mikropiiri), mistä seurasi yhteensopivuusogelmia. Nämä muutokset tehtiin Xilinx ISE -ohjelmistolla.

Laitteiston testauksen yhteydessä havaittiin häiriösignaali, jonka poistaminen vaatii lisätestausta. Laitteistolle tullaan tekemään tarvittavat muutokset testitulosten perusteella. Lopputuloksena emolevy päivitettiin onnistuneesti, tehtiin useita testauksia laitteistolle sekä päivityksiä firmwareen.

Avainsanat
SuperKEKB, Belle II, Instrumentation Delevopment Lab (IDLab), STURM2, X-ray beam profile monitor

Julkinen

SAVONIA UNIVERSITY OF APPLIED SCIENCES **THESIS**
Abstract

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Abstract

The purpose of this thesis was to update the motherboard and the firmware of the X-ray beam profile monitor and to do the needed testing. The work was done for the Instrumental Development Laboratory in University of Hawaii at Manoa. When the device is complete it will be placed to the Belle II detector located in KEK's (The High Energy Accelerator Research Organization) laboratory at Tsukuba, Japan. This is a part of SuperKEKB upgrade, which will bring the world's highest luminosity ($8x10^{35}$ $cm^{-2}s^{-1}$) for the KEK's particle accelerator.

The monitoring device includes the motherboard, 128 amplifiers, eight daughter cards and a firmware board for transferring the data. The motherboard needed some updates and those were done using the circuit board design software called PADS. Amplifiers were tested using the network analyzer and oscilloscope. The existing firmware was not fully functional and because the firmware board was changed also the FPGA (Field Programmable Gate Array) was altered and this caused compatibility problems. These modifications were done using Xilinx ISE.

While working with the device testing, noise signal was discovered. This signal needs further testing. Changes that need to be done for the device will be done according to the test results. As a result of this thesis the motherboard was updated successfully as well as many testing and firmware updates were made.

Keywords
SuperKEKB, Belle II, Instrumentation Delevopment Lab (IDLab), STURM2, X-ray beam profile monitor

Public

PREFACE

This thesis was made for Instrumentation Development Laboratory in University of Hawai'i at Manoa in Astronomy and Physics Department between January 2012 and July 2012.

I would like to thank Dr. Gary Varner for giving this opportunity to work in IDLab and to write my thesis on this project. I would also like to thank my supervisor, Ari Suopelto, for his support and help.

Kuopio February 20, 2013

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Janne Himanen

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SYMBOLS, CONCEPTS AND ABBREVIATIONS

ATF	Advanced Accelerator Test Facility
ASIC	Application Specific Integrated Circuit
BELLE	Detector located at the collision point at KEKB particle accelerator
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DFM	Design for Manufacturing
FEL	Free Electron Laser
FPGA	Field Programmable Gate Array
Mil	Unit of length measurement, one mil is thousandth of an inch
PADS	PCB design software from Mentor Graphics
PCB	Printed Circuit Board
RF	Radio Frequency
SCROD	FPGA firmware + PC software to control and readout waveform sampling ASICs for instrumenting sub detectors in high-energy physics experiments
STURM	Sampler of Transients for the Uniformly Redundant Mask
TSA	Timing Strobe Activate
VSWR	Voltage Standing Wave Ratio

1 INTRODUCTION

This thesis introduces some updates on the existing device, which has been developed to monitor X-ray beam. The monitoring device consists of a motherboard, 192 amplifiers, eight daughter cards and a SCROD board. The motherboard takes all the other components on it. Daughter cards are to digitize the amplified analog input signal. The SCROD board is used to connect the device to the computer and to communicate with ASICs (Application Specific Integrated Circuit) that are placed on the daughter cards. The FPGA chip and a firmware are placed on the SCROD. The project has three main focus areas: updating and testing the motherboard, testing the amplifiers and updating the firmware for the device.

2 PROJECT BACKGROUND

This project consists of the deployment of a novel, new X-ray monitor system for next generation lepton collider machines. These advanced accelerators utilize nanometer sized beam bunches. Monitoring consists of three key components: a fast sensor with RF amplification, a digitizer handling tens to hundreds of giga-samples per second and a fast acquisition back-end.

This real-time monitor system is an important component for the SuperKEKB upgrade. It will deliver the world's highest luminosity ($8x10^{35}$ $cm^{-2}s^{-1}$.) to the upgraded Belle II detector at the KEK High Energy Physics Laboratory in Tsukuba, Japan (Figure 1). The Belle II upgrade will allow searching for physics beyond the standard model of particle physics and continue the measurements of charge-parity violation, which confirmed the theory of Kobayashi and Maskawa. (Flanagan et.al. 2010, 1.)

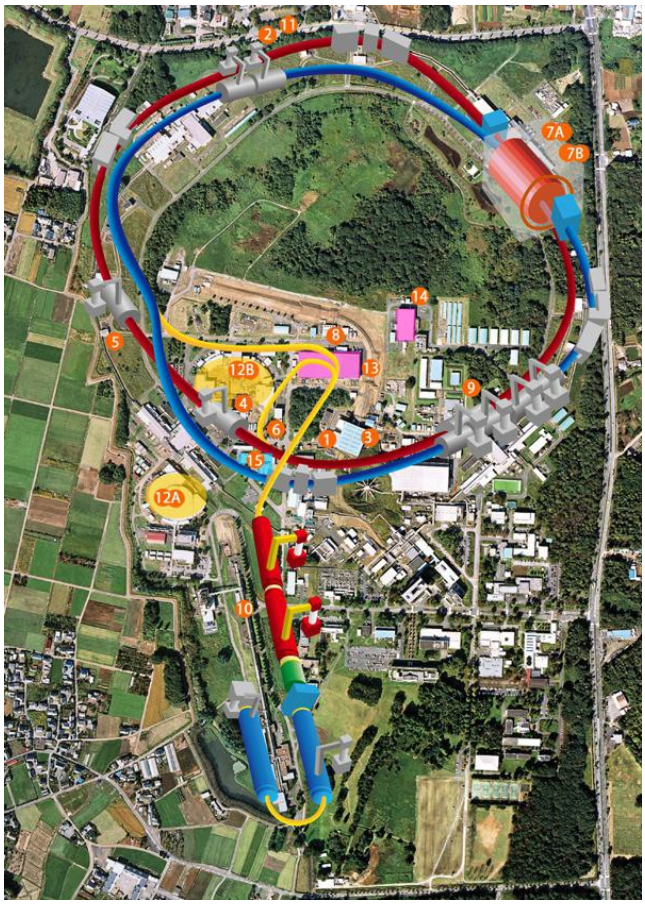

FIGURE 1. KEK Facilities and components in Tsukuba (Malin 2012, 8)

3 REQUIREMENTS AND OBJECTIVES

The device uses a fermionics sensor as an input. The X-ray signal coming to the sensor is estimated to be 3.6 keV. The energy needed to release one electron-hole pair from silicon is 3.6 eV; the estimated signal produces 1,000 electron-hole pairs. One electron has a charge of 1.6021773 * 10^{-19} C so 1,000 electron hole-pairs have a charge of about 0.16 fC. This basic operating principle is illustrated in Figure 2. (Instrumentation Development Laboratory 2010a, 1.)

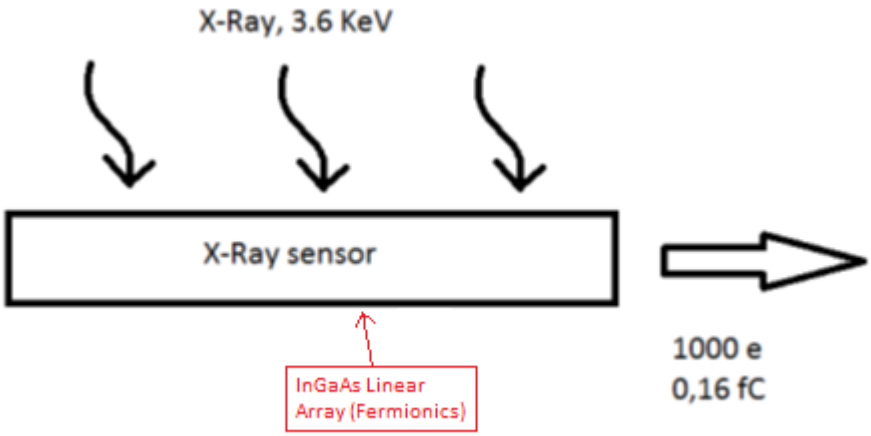

FIGURE 2. Sensor's basic operating principle (Instrumentation Development Laboratory 2010a, 1)

The response time for the sensor is 0.5 ns and signal's low to high change time, Δt, is 0.25 s. Within the low to high change time the sensor produces the current of

$$\Delta I = \frac{\Delta q}{\Delta t} = \frac{0.16 * 10^{15}\ C}{0.25 * 10^{9}\ s} \approx 0.7\ \mu A \quad (1)$$

With the 50 Ω transfer line, the sensor's output voltage is

$$\Delta V = \Delta I * R = 0.7\ \mu A * 50\ \Omega \approx 35\ \mu V \quad (2)$$

At least 10 mV output voltage is needed to get a reasonable resolution. When the input signal for the fermionics sensor is about 35 µV, the total gain is

$$G = 20 * log_{10} \frac{U_{out}}{U_{in}} = 20 * log_{10} \frac{10m\ V}{35\ \mu V} \approx 50\ dB \quad (3)$$

(Instrumentation Development Laboratory 2010a, 2-3.)

4 MOTHERBOARD ARCHITECTURE

The main function of the motherboard is to connect all other components of the device together. The dimensions of the motherboard are 10.9 X 12 inches. The fermionics sensor is connected to the motherboard with a CPG18020 PGA socket, which uses simple lever. Input from the sensor goes through three amplifier stages and there are low pass filters between the stages. Filters are needed to reject unwanted high frequencies. After the signal is amplified with a total of 60 dBs it goes to the ASIC card (daughter card). This is where the analog-to-digital conversion happens. Finally, the signal goes to SCROD from where the signal is transferred to the computer. The block diagram is seen in Figure 3. (Malin, 2011, 2.)

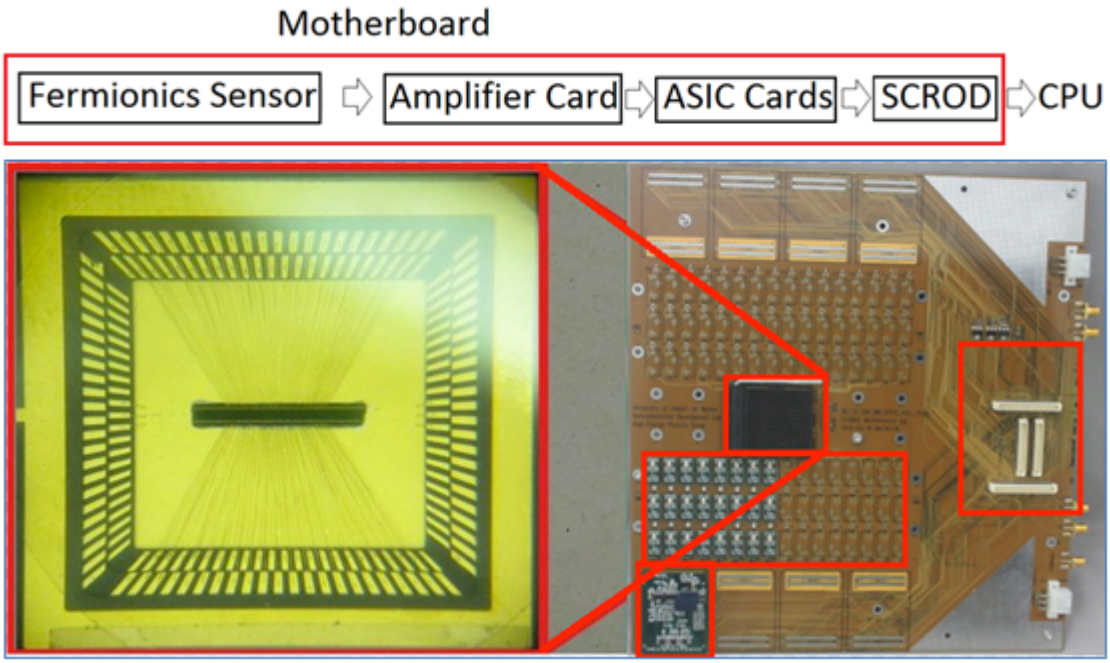

FIGURE 3. Motherboard block diagram (2012)

The fermionics sensor has 64 detectors for measuring X-ray beams and therefore there are eight daughter cards. All daughter cards are placed on top of the motherboard. Every daughter card can handle eight channels and every channel needs three amplifiers so the total amount of amplifiers is 192. Amplifiers are placed on both sides of the motherboard (IMAGE 1). The estimated power consumption of the motherboard is 30W and that is why there are four ground planes (two on top and two on bottom layer) for cooling the board. (Malin 2011, 2 & 5.)

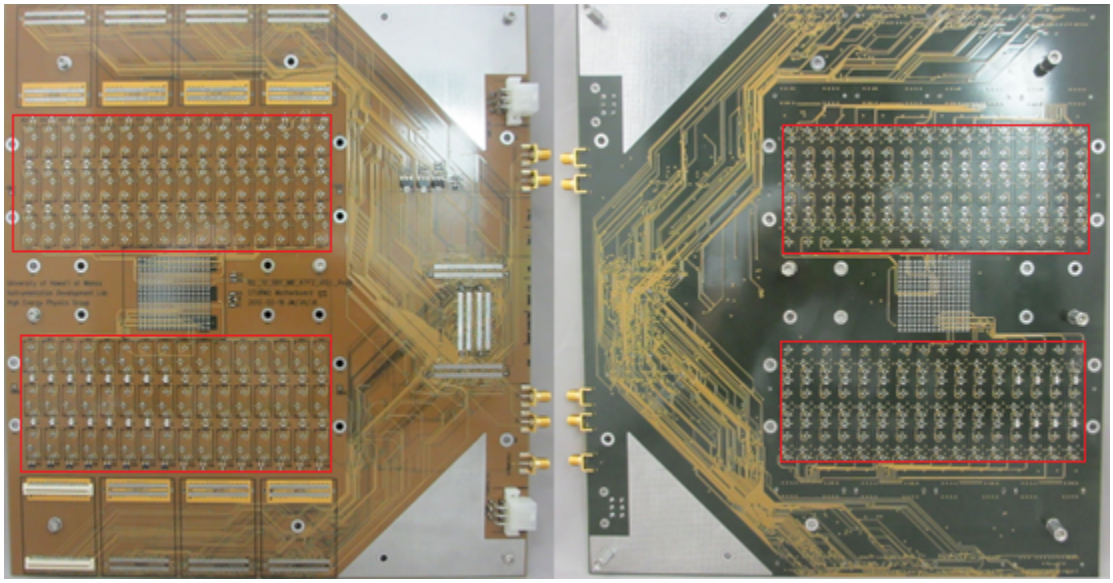

IMAGE 1. Amplifiers' positions on motherboard top (left) and bottom (right)

All the connectors used to make the connections outside the motherboard are on the right side of the motherboard and they are located in the middle of Image 1. There are two 6-pin molex power connectors for the five volt power supply and five SMA connectors (three of those for debugging, one for SCROD's common clock and one for fermionics sensor's down bonds). (Malin 2011, 3-4.)

4.1 PCB design

In this project PADS from Mentor Graphics was used for PCB designing. PADS has three different modules: layout, logic and router. Layout and router are used for designing layout and routing. Logic is used to make schematics.

There are three phases while making a PBC design. The first thing is to make schematics by using PADS Logic. In this part all used components are chosen and connections are made. After that the layout must be created. The first thing to do is to import all components to the layout. This happens by outputting a netlist to the PADS Layout. This imports all components which have a footprint. At this point components are not routed but connections can be seen. If components do not have footprints they must be created. Most common components have footprints created already but right libraries needs to be imported to the PADS to assign them. When all components have footprints they are placed as wanted on the PCB and routed together using PADS Layout, PADS Router or both. Finally design rules must be checked and the design must be verified. PADS Layout has an operation to verify the design. This checks if the board is theoretically possible to manufacture by checking the following parameters:

- Clearance
- Connectivity
- High speed
- Maximum via count
- Plane
- Test points
- Fabrication
- Latium design verification
- Wire bonds

The most important design rules in this project are the clearance rules (Figure 4), which tell the widths for all parts of the PCB. The clearance rules remained the same as in the first version of the motherboard.

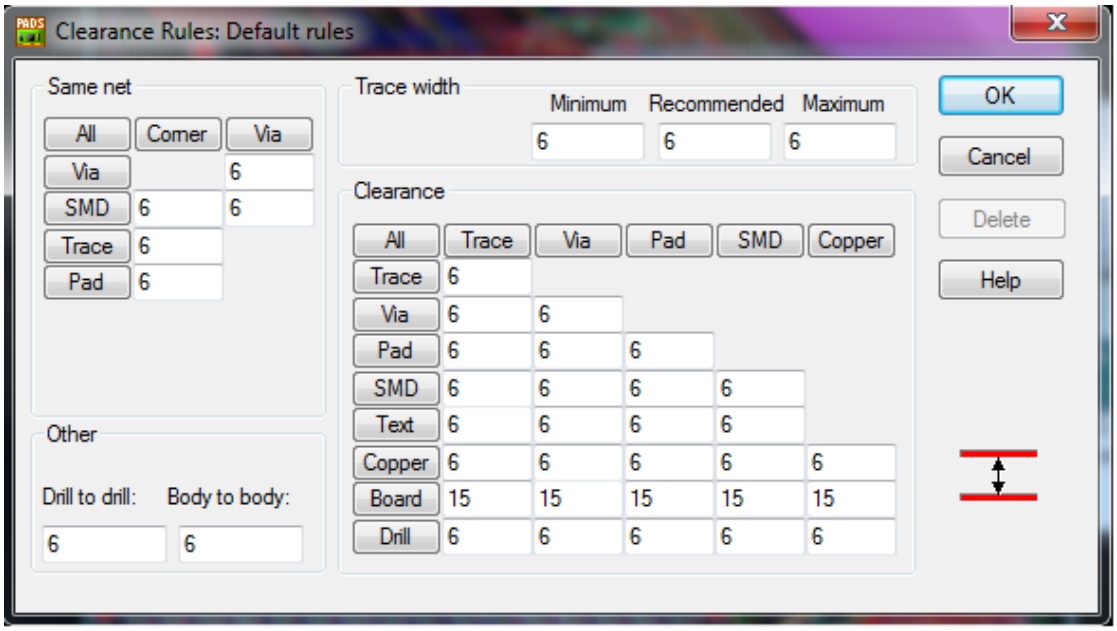

FIGURE 4 Clearance rules

The next thing to do is to generate the artwork to Gerber files. These files are needed to fabricate the circuit board and also to do DFM (Design for Manufacturing) check. After the design passes the DFM check the board is ready to be fabricated.

After the board has been fabricated is must be tested. This part is very important since if some trace has a cut, the board is not going to work like wanted. This happens simply by using multimeter to test the continuity of the traces.

4.2 Updates

The motherboard has two different revisions (revA and revB). They both include the same basic idea but there were some problems in revA which are corrected in revB. The first thing corrected was the wrong footprint in the 80-pin connector where the daughter card stands on. In PADS it is possible to choose between three different units: inches, millimeters and mils (mil is a thousandth of an inch). The problem in revA was the confusion between mils and millimeters. The pitch between the pads should have been 0.80mm but they were actually 0.7874mm (Figure 5). After the correction some of the motherboard's traces overlapped and needed to be rerouted.

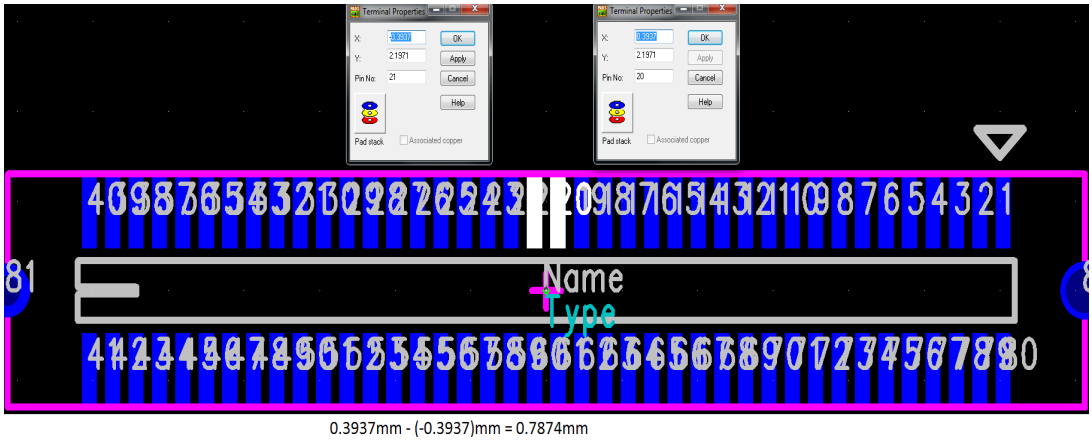

FIGURE 5. Connector's footprint was wrong

At different parts of the motherboard many voltage levels are used and because of this operating voltage needs regulation. Right next to the CPG18020 socket, the VPED voltage is regulated from 5 V to 2.5 V. The VPED voltage is used in the sensor to make it more stable. revA uses a LT3020EDD regulator, which has nine pins and needs two resistors and one capacitor. In revB it was changed to a AP7333 which has only three pins and therefore it is much simpler to route and only two capacitors are needed (Figure 6).

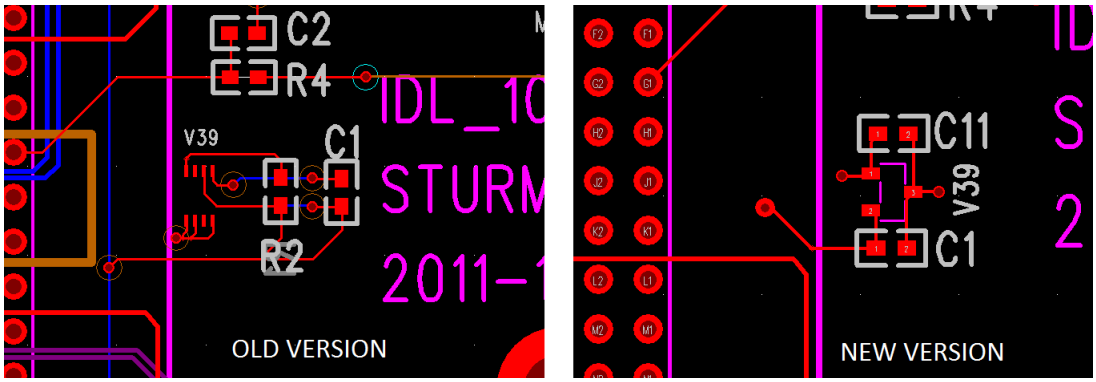

FIGURE 6. Regulator was changed for a simpler one

On the right side of the motherboard there are two cooling areas but in revA one top solder mask was missing so it was added to revB. Both cooling areas are filled with vias so it cools out all layers of the board. In revA also more vias were added to make it more reliable (Figure 7).

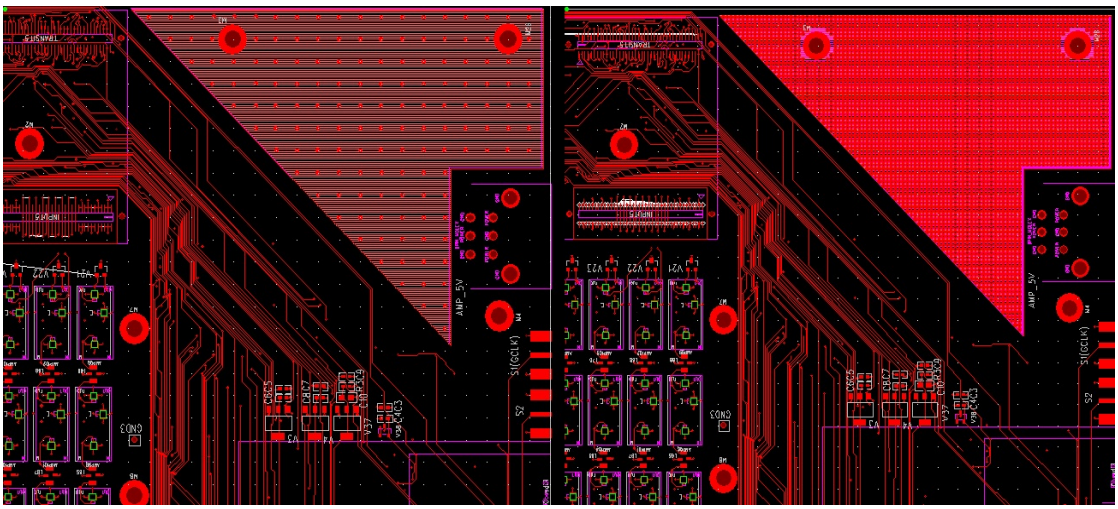

FIGURE 7. Part of the motherboard's top solder mask was missing and more vias were added

The motherboard takes its operating voltage through a 6-pin molex connector. This connector has three pins for ground and three pins for power. In revA power pins' functions were grounds and vice versa (Figure 8).

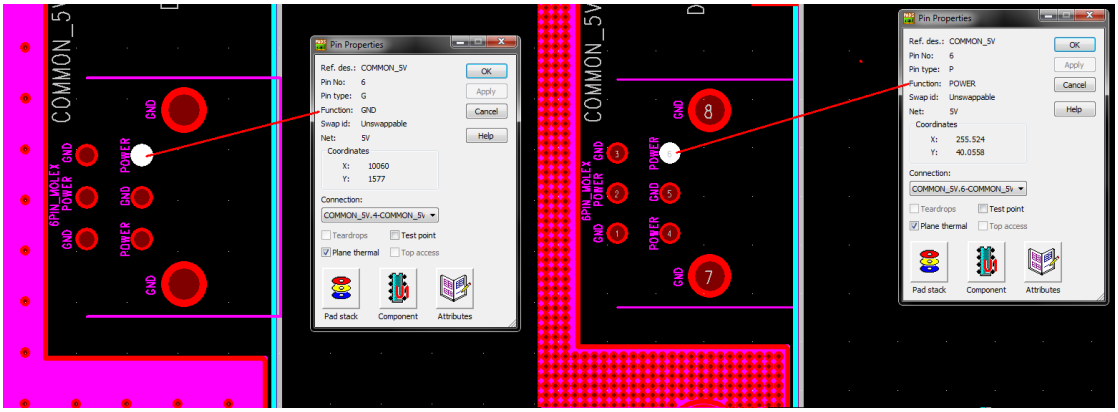

FIGURE 8. Power connector with wrong functions (left) and corrected one (right)

5 AMPLIFIER CARD

The basic operation of the amplifier is seen in Figure 9. The amplifier card uses an ABA-31563 amplifier, which produces 21.5 dB gain. The attenuator (LAT-2+) is used to reduce the unwanted reflected signal. The voltage is regulated with an NCP583 regulator from four volts to three volts. The amplifier card is connected to the mother-board with three MHF4P RF connectors. The assembled amplifier is seen in Image 2.

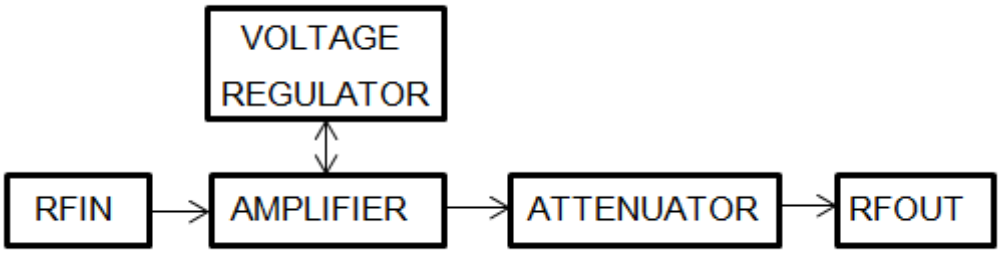

FIGURE 9. Amplifier's block diagram

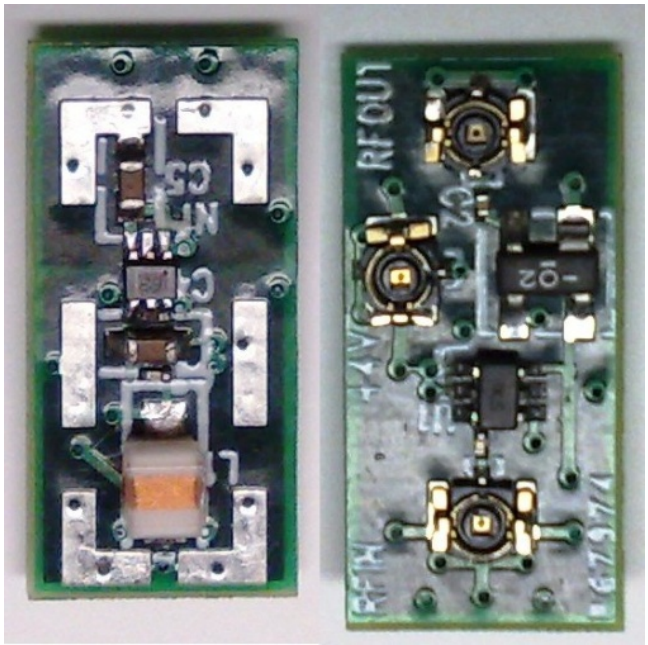

IMAGE 2. Amplifier card top (left) and bottom (right)

The amplifier carrier card (Image 3) was designed to make testing easier. There are three SMA connectors. Two of those are to connect the signal in and out. The third connector is for a four volt power supply. The carrier card uses same kind of con-nectors for connecting amplifier as the motherboard.

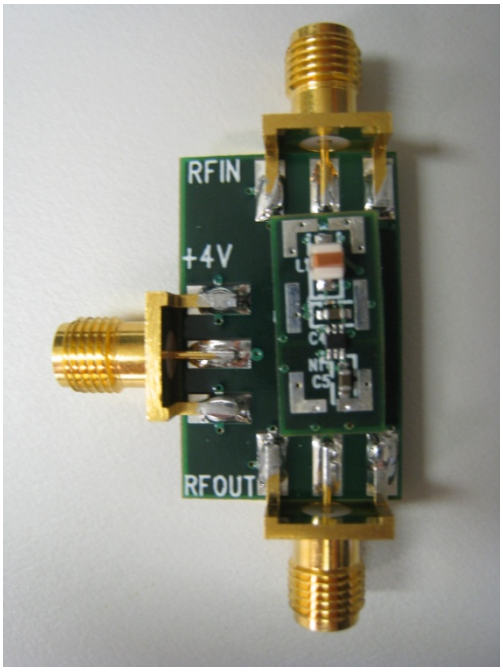

IMAGE 3. Amplifier carrier card

5.1 Testing

Amplifier tests were done with Agilent N9923A FieldFox RF Vector Network Analyzer (Image 4). This network analyzer has a frequency rate of 2 MHz to 6 GHz and it is used to measure scattering parameters (S-parameters). This analyzer uses two ports so it is possible to measure magnitude and phase for S11, S21, S22 and S12. Gain was only interesting parameter at this situation so the magnitude of the S21 was measured. S12 is meant for measuring attenuation and S11 and S22 tells the ports reflections. (Agilent Technologies 2012, 8 & 21-22.)

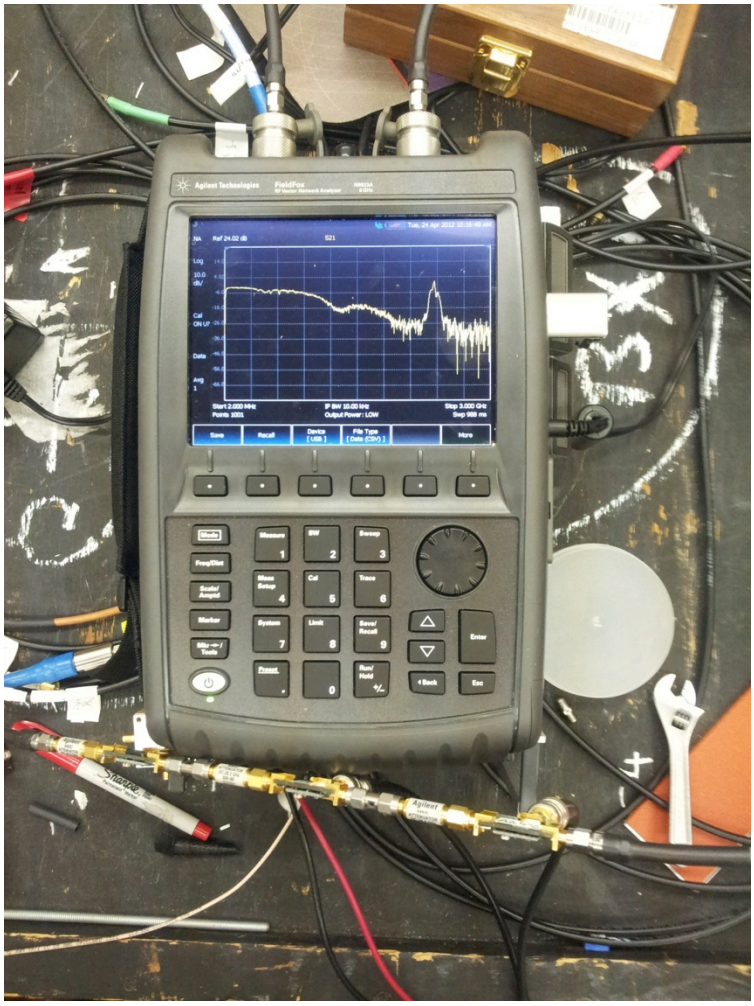

IMAGE 4. Agilent N9923A FieldFox RF Vector Network Analyzer

Before using this network analyzer it needed to be calibrated. This calibration was integrated into the analyzer. With this calibration the use of high quality cables and components is very important. The calibrating process was really simple. Open, short and load connectors are connected by turns to port one and port two and the analyzer makes sweeps and corrects all the S-parameters. (Agilent Technologies 2012, 69-73.)

After calibration all 25 assembled amplifiers were tested individually with the carrier board (Image 5). Because amplifiers were supposed to have 20 dB gain, 20 dB attenuator was connected in series with the amplifier to protect the analyzer. Test results are seen in Figure 10.

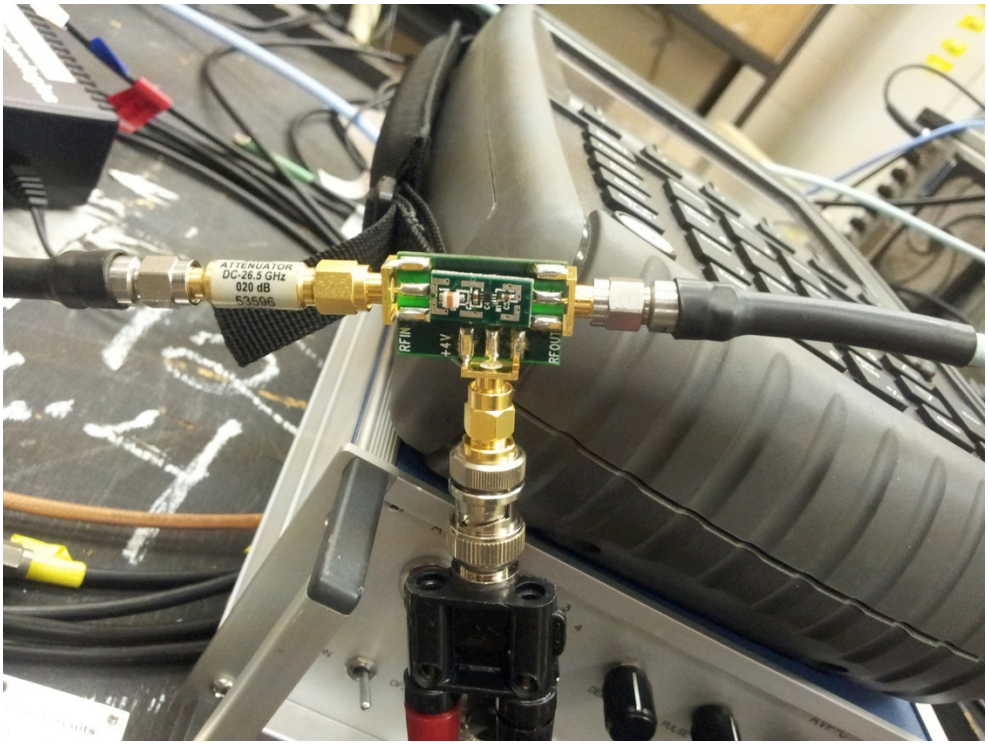

IMAGE 5. Individual amplifier test connection

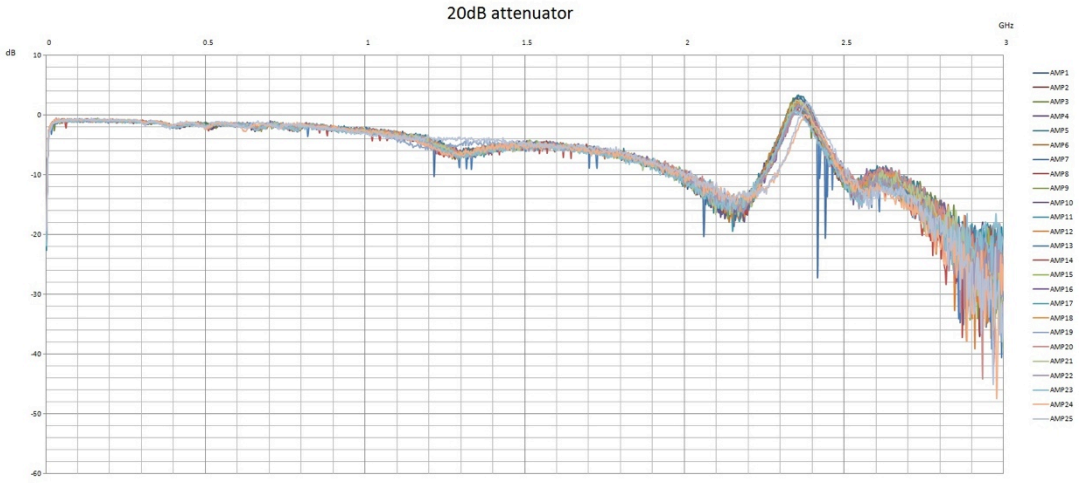

FIGURE 10. Results for individual amplifier tests

After individual tests the amplifiers were connected in series of three (Image 6). At this time the total gain was supposed to be 60 dBs and therefore three 20 dB attenuators were used as a protection. The results are seen in Figure 11.

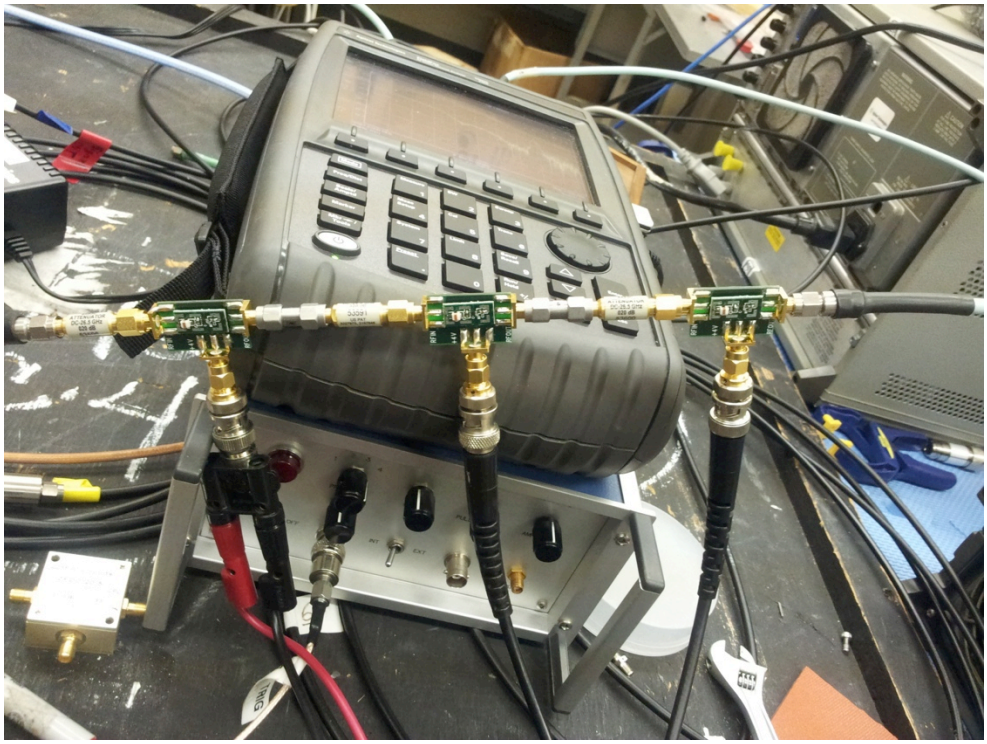

IMAGE 6. Connection for the amplifier test in series of three

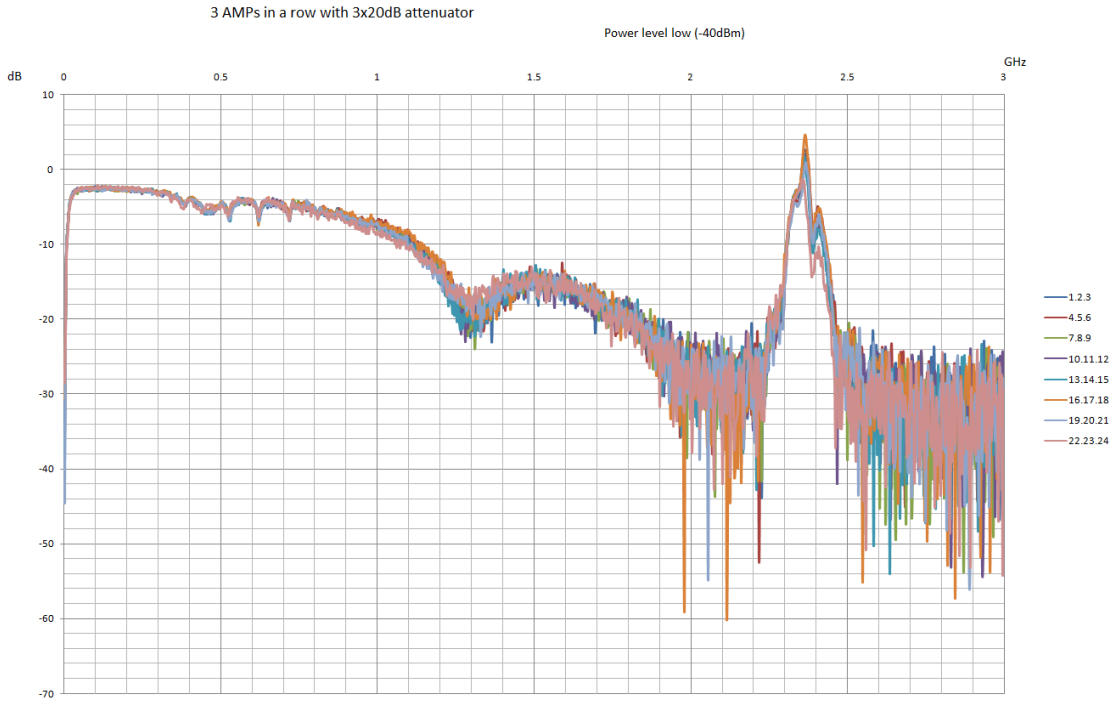

FIGURE 11. Results for the amplifiers in series of three

As seen in both figures (Figure 10 and Figure 11) the gain level is near 0 dB like it is supposed to be since in both situations the attenuation levels are the same as the total gain. In this project the interesting frequency level is around 1 GHz so the gain is rather linear at this point. The spike seen around 2.5 GHz was tried to be eliminated with filters on the motherboard.

The third phase of the amplifier tests was putting the amplifiers on the motherboard. Eight channels were used for testing. Instead of using the fermionics sensor, signal generator (Agilent E4432B) was used. A testing board needed to be made to connect signal generator to the PGA socket. The testing board has pins for the signal and the ground and one SMA connector to connect the signal generator to simulate the input signal. The output signal was taken out for the oscilloscope by using modified daughter card. The modifier daughter card has eight SMA connectors, which are connected to take the amplified signal for the oscilloscope (Agilent 54641D). The testing set-up can be seen in Image 7 and the testing boards in Image 8.

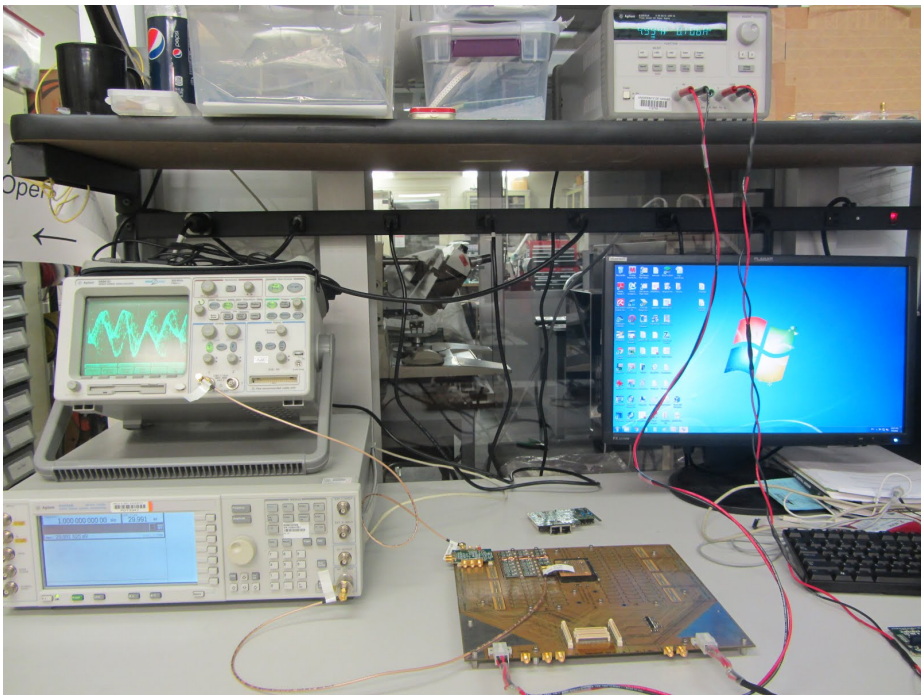

IMAGE 7. Testing set-up

5.2 Oscillation

When using almost any kind of input signal lots of oscillation was received. The first flaw noticed was a wrong kind of filter between the amplifier stages. An LFCN-1325 low pass filter was chosen since it passes all frequencies below 1325 MHz but instead of absorbing the higher frequencies it reflected them back and caused oscillation. One important thing to notice was that after about 1.3 GHz VSWR (voltage standing wave ratio) value increases dramatically. Ideal value for the VSWR would be 1.0. This means that there is no unwanted reflecting signal. But in this case VSWR goes up to 3.9 in 1.5 GHz and over 30 after 2 GHz. Ideal filter could not be found so at one channel both filters were removed but it did not remove all of the oscillation. (Mini-Circuits, 2013, 1.)

The second thing to try was to increase the attenuation on the amplifier cards. Originally the amplifier cards have LAT-2+ fixed attenuators, which causes an attenuation of about two decibels. The attenuation was increased all the way to five decibels by using LAT-5+ fixed attenuators but it made a minimal change and at this point the amplification was too small.

Shielding the amplifiers could help remove problems coming through the air. Shielding one channel with aluminum tape (Image 8) was tried but it was not strong enough to cause any changes for the oscillation.

The last thing to try was to remove part of the amplifier stages only to test if it helps. This was done by replacing some of the amplifier stages with “dummy boards” (board without amplification). This test was done by using only one channel. As a result it was clearly seen that taking away part of the amplifiers made noise signal much smaller but it did not completely remove it. Even without any input signal some noise was received. This is because the device is very delicate to outside disturbance and the test boards were not ideal.

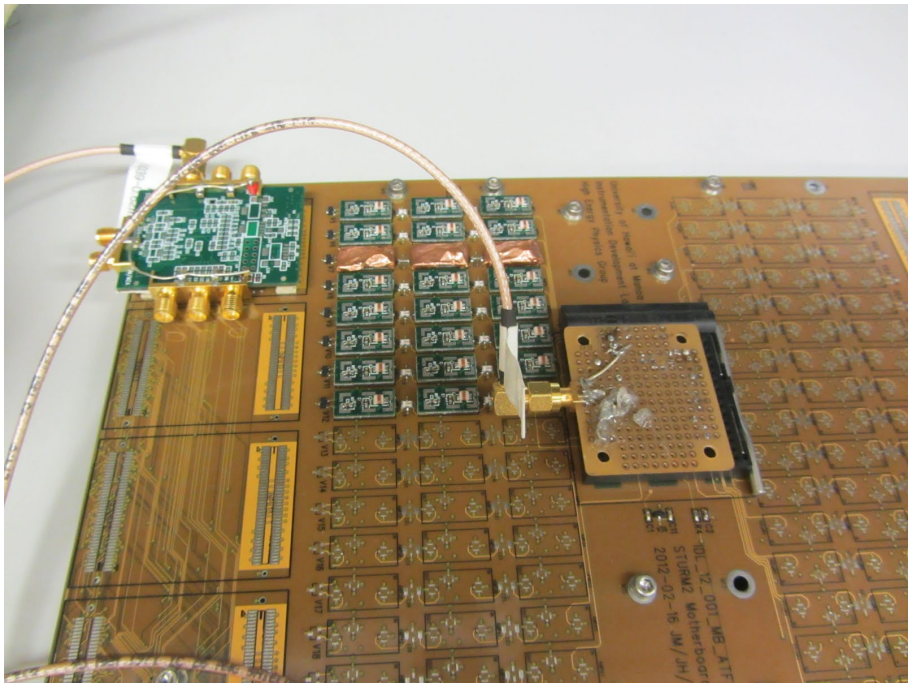

IMAGE 8. Problem solving set-up

6 DAUGHTER CARD

After amplifier stages the signal goes to the daughter cards (Image 9). The mother-board holds eight daughter cards with two 80-pin connectors and each of those takes in eight RF channels. Every daughter card holds the STURM2 ASIC chip, which takes samples and digitalizes the analog signal. At the end, the signal is transferred to the SCROD board (FPGA board). The block diagram of the daughter card is seen in Figure 12. (Instrumentation Development Laboratory 2010b, 1-2.)

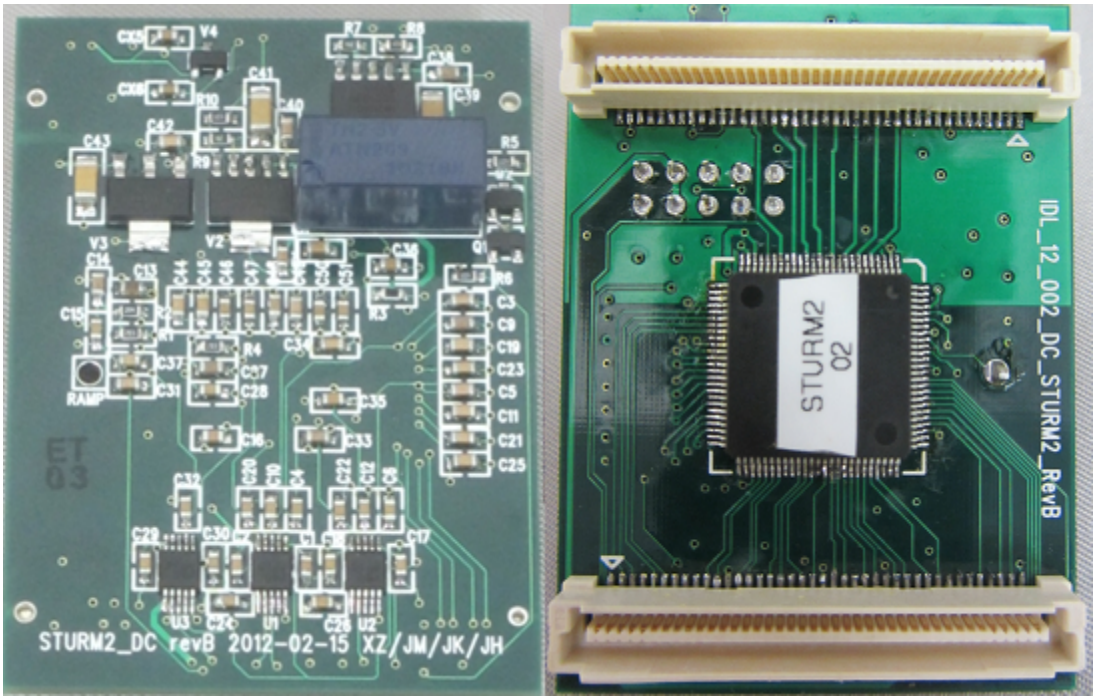

IMAGE 9. Daughter card top (left) and bottom (right)

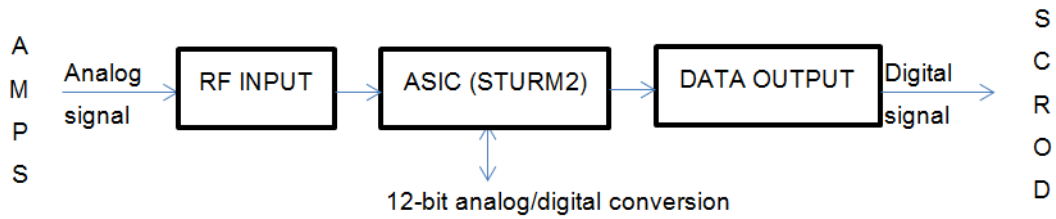

FIGURE 12. Daughter card's block diagram

7 STURM2 CHIP

STURM2 is an ASIC chip, which is fabricated specifically for this project. It is used for making a 12-bit analog-to-digital conversion with fast sampling speed (1-200 gigasamples/second). To be able to reach such speed its every channel converts the samples in parallel instead of doing it sequentially. The STURM2 is based on the former STURM chip, which was slower and had an unstable ADC (analog to digital conversion). Some fine tune was made also for its sample-timing control and RF input. The sampling speed can be calculated with the following equation where n stands for the number of the samples. (Varner 2009, 14.)

$$Sampling\ speed = 1 + n * 0.02\mu s \quad (4)$$

As seen on the blog diagram (Figure 13), STURM2 has eight sampling channels and one monitoring channel. For sampling control it has four TSA buffers and eight DAC controllable delays. Every buffer takes eight samples so there are 32 channels. Data is stored at the storage array, which consists of 288 Wilkinson conversion cells. (Varner 2009, 14.)

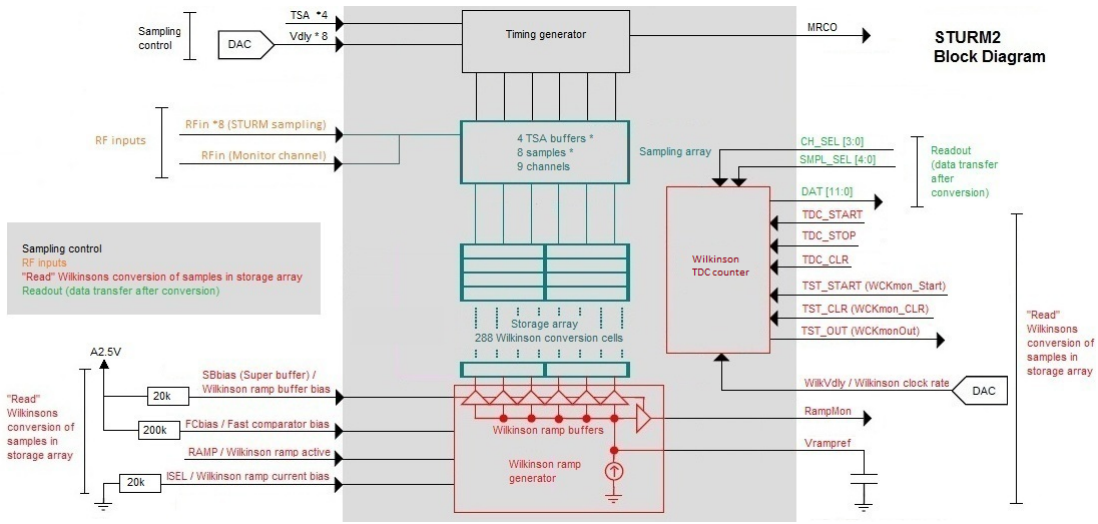

FIGURE 13. STURM2 block diagram

Data is read for conversion from storage array through the “read” module. It is possible to monitor ramp with oscilloscope to test if it works properly. The clock rate of the ADC can be changed through DAC. The “readout” module is used as an output for the data after the conversion.

8 FIRMWARE

The first version of the firmware was implemented to work with STURM2Eval evaluation board (Image 10), which has been designed just for this project. This board uses Linux based software called USB Tester but since the final device is using the SCROD board (Image 11), the firmware needed to be modified to be compatible for that. The STURM2Eval board uses Spartan 3 FPGA and the SCROD uses Spartan 6 and that is why many changes were needed.

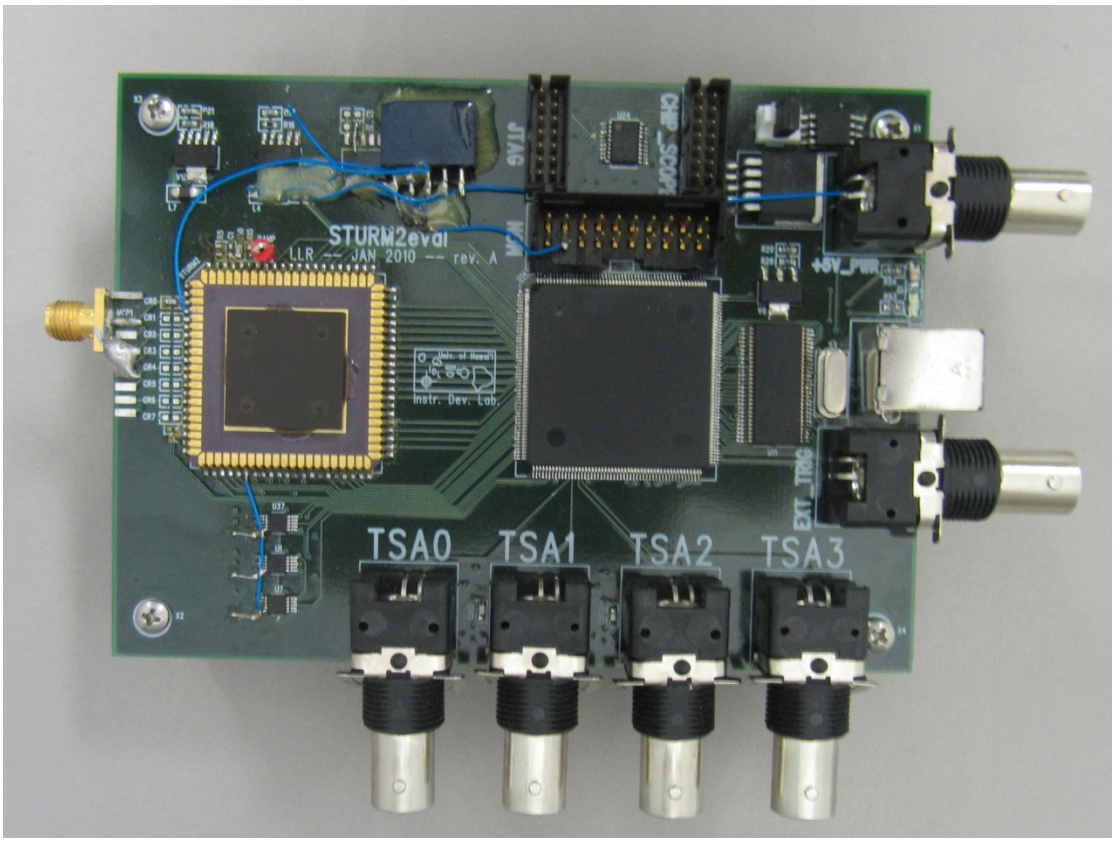

IMAGE 10. STURM2Eval evaluation board

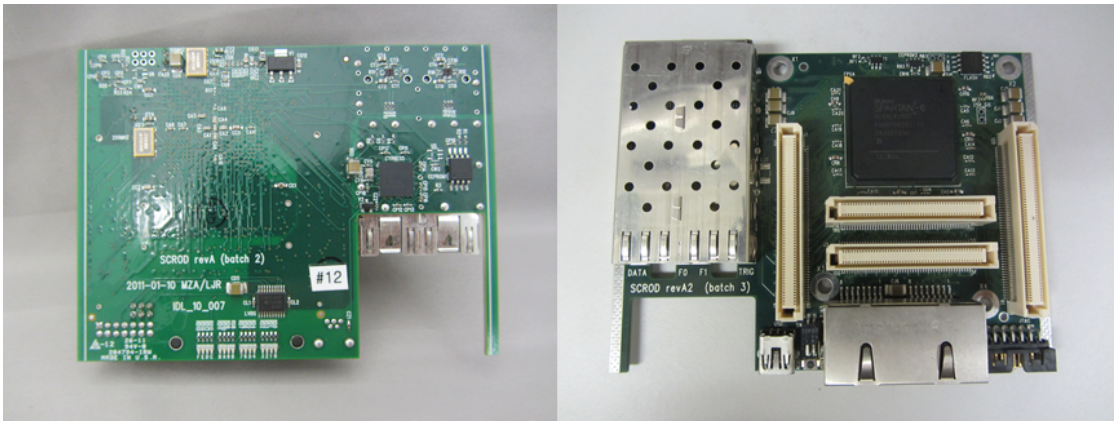

IMAGE 11. SCROD board bottom (left) and top (right)

8.1 Firmware architecture

The TOP module is at the highest place in the firmware hierarchy. The TOP module is divided to four different main modules, which are CLK, USB, STURM2 and DAC. These main modules share signals between each other and they communicate through the TOP module as seen in Figure 14. The TOP module is connected to the pins of the FPGA. The pin connections are defined in the UCF file, which is seen in Appendix 4.

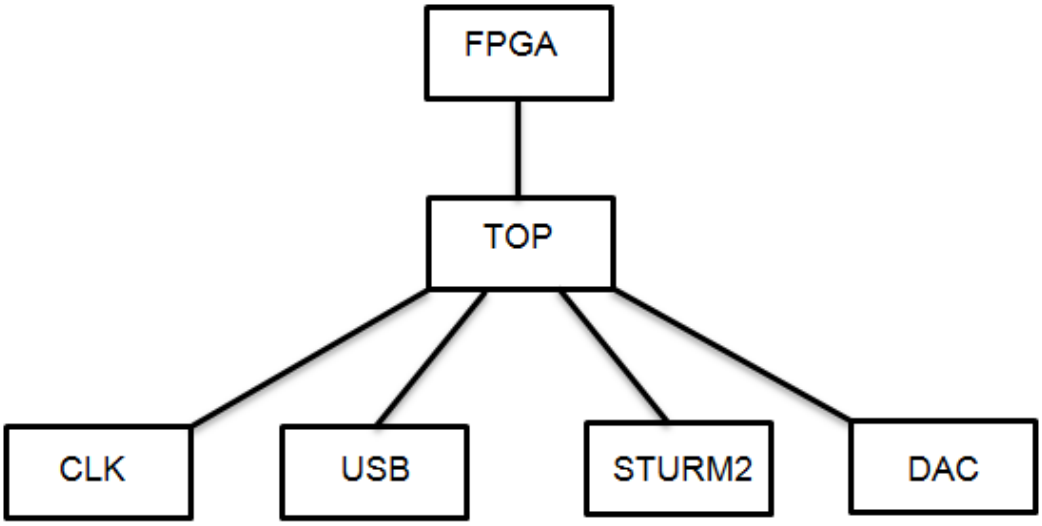

FIGURE 14. Firmware architecture

The CLK module takes the base clock signal from the FPGA through the TOP module. Original Spartan 3 FPGA has the 150 MHz base clock signal, which was divided to other signals by using the DCM (Digital Clock Manager). The DCM was made by writing it down as a normal HDL code (Figure 15). Spartan 6 FPGA has 250 MHz base clock and it does not support DCM. This is why the new code uses Clocking Wizard (Figure 16) to produce the needed clock signals from the base signal. Clocking Wizard is a core, which produces the code by the settings put into the core. Buffers for the signals can also be produced in Clocking Wizard core as seen in Figure 17.

```
xDCM : DCM
generic map(
   CLKIN_PERIOD => 6.667,
   CLKIN_DIVIDE_BY_2 => true,
   CLKDV_DIVIDE => 7.5)
port map(
   CLK0     => CLK0,
   CLK180   => open,
   CLK270   => open,
   CLK2X    => open,
   CLK2X180 => open,
   CLK90    => open,
   CLKDV    => CLKDV,
   CLKFX    => open,
   CLKFX180 => open,
   LOCKED   => LOCKED,
   PSDONE   => open,
   STATUS   => open,
   CLKFB    => CLKFB,
   CLKIN    => CLK,
   DSSEN    => '0',
   PSCLK    => '0',
   PSEN     => '0',
   PSINCDEC => '0',
   RST      => xCLR_ALL);
```

FIGURE 15. Old DCM

```
xCLK_WIZ :  CLK_WIZ
port map(
BCLK_P      =>    BCLK_P,
BCLK_N      =>    BCLK_N,
RST         =>    not(xWAKEUP),
CLK_150MHz  =>    xCLK,
CLK_10MHz   =>    xCLK_10MHz,
CLK_75MHz   =>    xCLK_75MHz,
LOCKED      =>    LOCKED
);
```

FIGURE 16. New Clocking Wizard

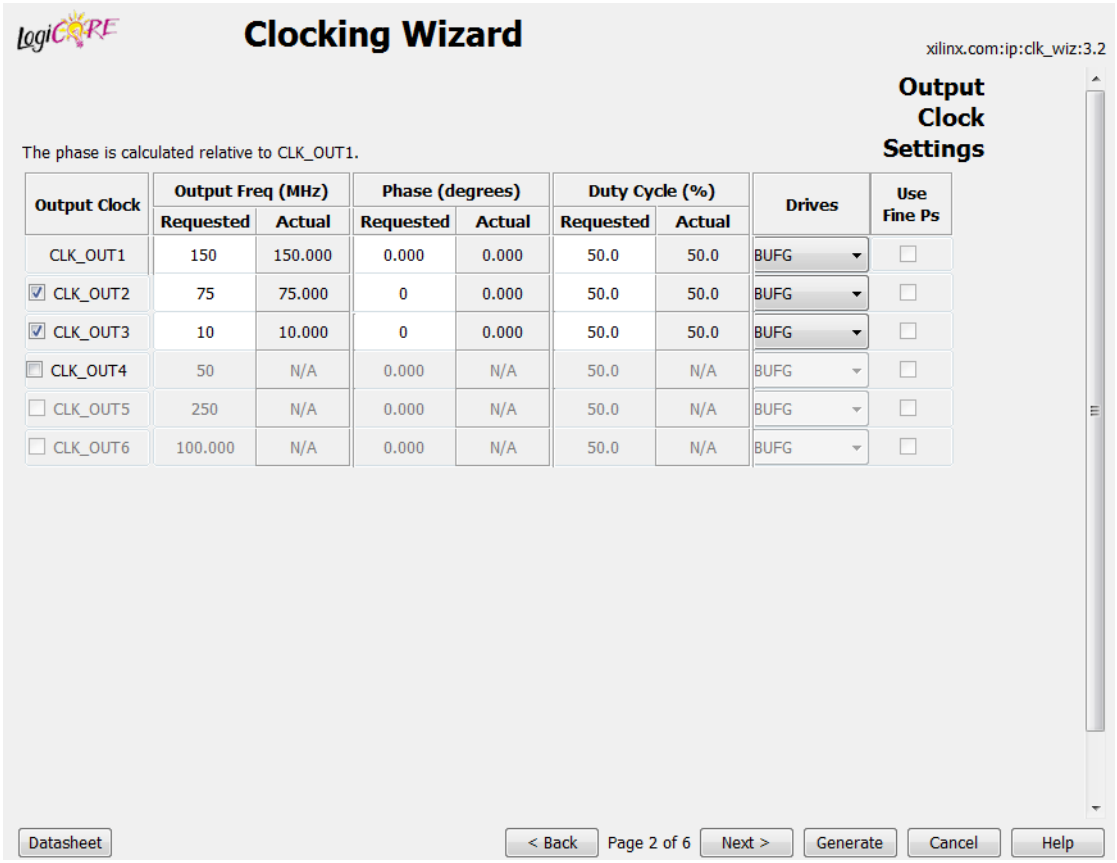

FIGURE 17. Output clock signal settings in Clocking Wizard

In the DAC module it is possible to modify the delays to control timing for sampling and Wilkinson counter. The Wilkinson counter's start and clear operations and the output signal are also controlled in this module. The original code used OBUF for incoming clock signal. This is not possible anymore since the signal has been buffered already in the Clocking Wizard and using double buffer is not allowed. Now xCLK_10MHz signal is signed to be SCLK by using ODDR2 component. The original buffer can be seen in Figure 18 and the new component in Figure 19.

```
xOBUF_SCLK : OBUF
port map (
   I  => xCLK_10MHz,
   O  => SCLK);
```

FIGURE 18. Old buffer for SCLK

```
ODDR2_SCLK : ODDR2     -- instead of obuf
  generic map(
     DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
     INIT => 0, -- Sets initial state of the Q output to '0' or '1'
     SRTYPE => "SYNC") -- Specifies "SYNC" or "ASYNC" set/reset
  port map (
     Q => SCLK, -- 1-bit output data
     C0 => xCLK_10MHz, -- 1-bit clock input
     C1 => not (xCLK_10MHz), -- 1-bit clock input
     CE => '1',    -- 1-bit clock enable input
     D0 => '1',    -- 1-bit data input (associated with C0)
     D1 => '0',    -- 1-bit data input (associated with C1)
     R => '0',-- 1-bit reset input
     S => '1'      -- 1-bit set input
  );
```

FIGURE 19. New component to replace the buffer

8.2 Testing

While using the STURM2Eval board testing were made with the USB tester software, which is specifically made for this project and is running on Linux. Testing happened by taking samples out with the software and comparing if those respond to the input. Since the final version of the firmware is supposed to work on the SCROD, most of the tests were done with the SCROD. These tests were done by ChipScope, which is a logic analyzer integrated to the Xilinx ISE software. With the ChipScope it is possible to follow any signal and see how it varies. To do that, an "integrated controller" (ICON) and an "integrated logic analyzer" (ILA) are needed to be used. A "virtual input/output" (VIO) is used to simulate the trigger in the code. (Xilinx 2012, 11-17.)

The first and the most important thing noticed was that the main clock was not working. This is why the SCROD needed some changes mentioned below (8.3. Hardware changes). Also the changes made for the VDLY values were confirmed.

8.3 Hardware changes

While using the first version of the SCROD (revA) at the first time the main clock was not working. That is why the new version (revA2) was made. But before using the new version some changes needed to be done. At first a small piece of kapton tape was placed at the motherboard to work as an insulator. This was done because otherwise the shielding tabs of the RJ45 connectors would have contacted each other's. Other thing to do was replacing one resistor from 10 kΩ to 2.4 kΩ. This was done because without this change the FPGA does not look for a program on the SPI flash when booted. Also four different resistors were removed to make oscillators work. Finally an EEPROM (Electrically Erasable Programmable Read-Only Memory) needed to be changed to another one. Because the pins were not at the same positions as earlier some wires needed to be added as seen in Image 12. (Andrew 2012, 1.)

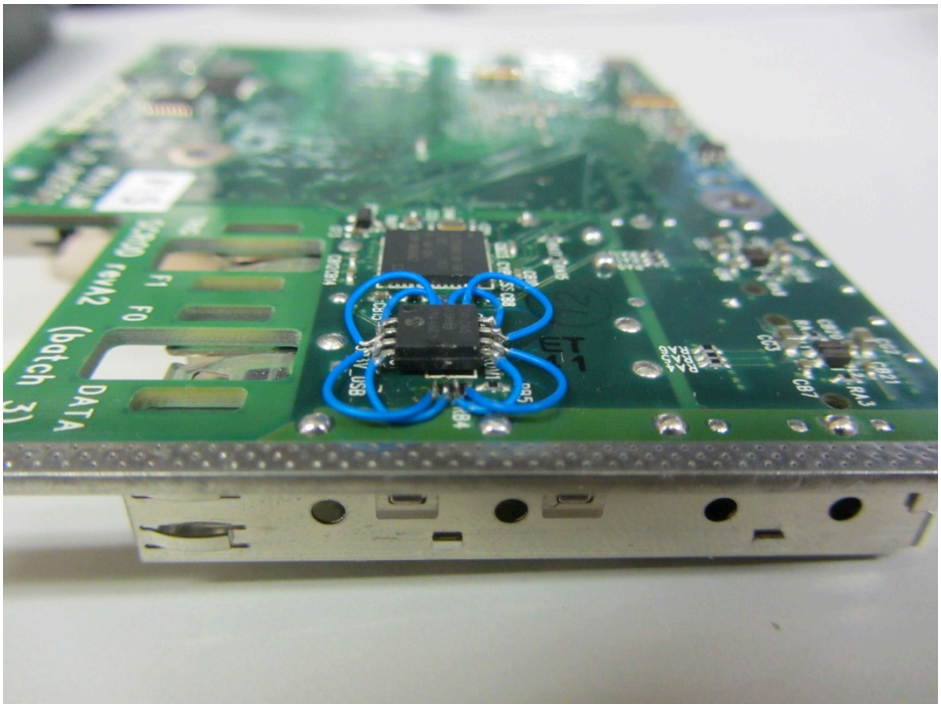

IMAGE 12. New EEPROM

9 RESULTS AND CONCLUSION

All the changes for the motherboard were made successfully and it works as wanted if thought as a standalone component. Also the amplifiers work as wanted when they are not connected to the motherboard. But when all components are attached together, plenty of noise is received. That is the reason why the device needs more testing and further development.

The biggest issue in the firmware was nonfunctional clock signal, which was corrected successfully. Some other minor corrections were made but still the firmware is not fully compatible with Spartan 6 FPGA. This is why also the firmware needs further development.

10 FURTHER DEVELOPMENT

The motherboard needs more testing while the amplifiers are attached on it since the aluminum tape did not provide enough shielding. The next phase would be to use stronger metal to block the noise signals releasing through the air. This was left undone because of the lack of time.

Equally, one major change in the layouts of the motherboard and the daughter cards could solve the oscillation problem. At the moment all amplification happens on the motherboard and from the beginning it was known that is might be an issue. If one stage of the amplifiers were moved on the daughter cards there would not be so much amplification on the same board. This would need new PCB designs for the motherboard and daughter cards. Some tests need to be done on the firmware to solve the compatibility problems.

Before testing the device in Tsukuba it should be tested at laboratory in Hawaii. The test-setup can be seen in Figure 20. At first, the free electron laser (FEL) is used to fire a microwave pulse. The pulse is bent with the infrared laser and optical storage cavity. When the pulse is bent it emits X-rays. When X-rays arrive at the collimator, intensity is measured. At last, the beam arrives at the detector and now it is possible to compare the results and make the final changes in the device.

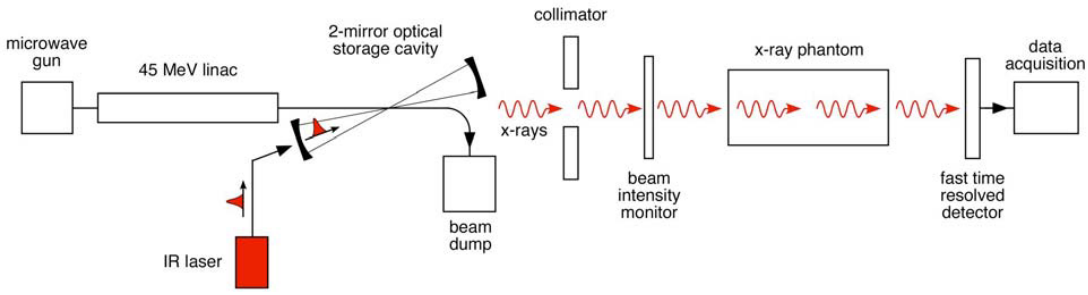

FIGURE 20. Test-setup for the device (Varner 2009, 11)

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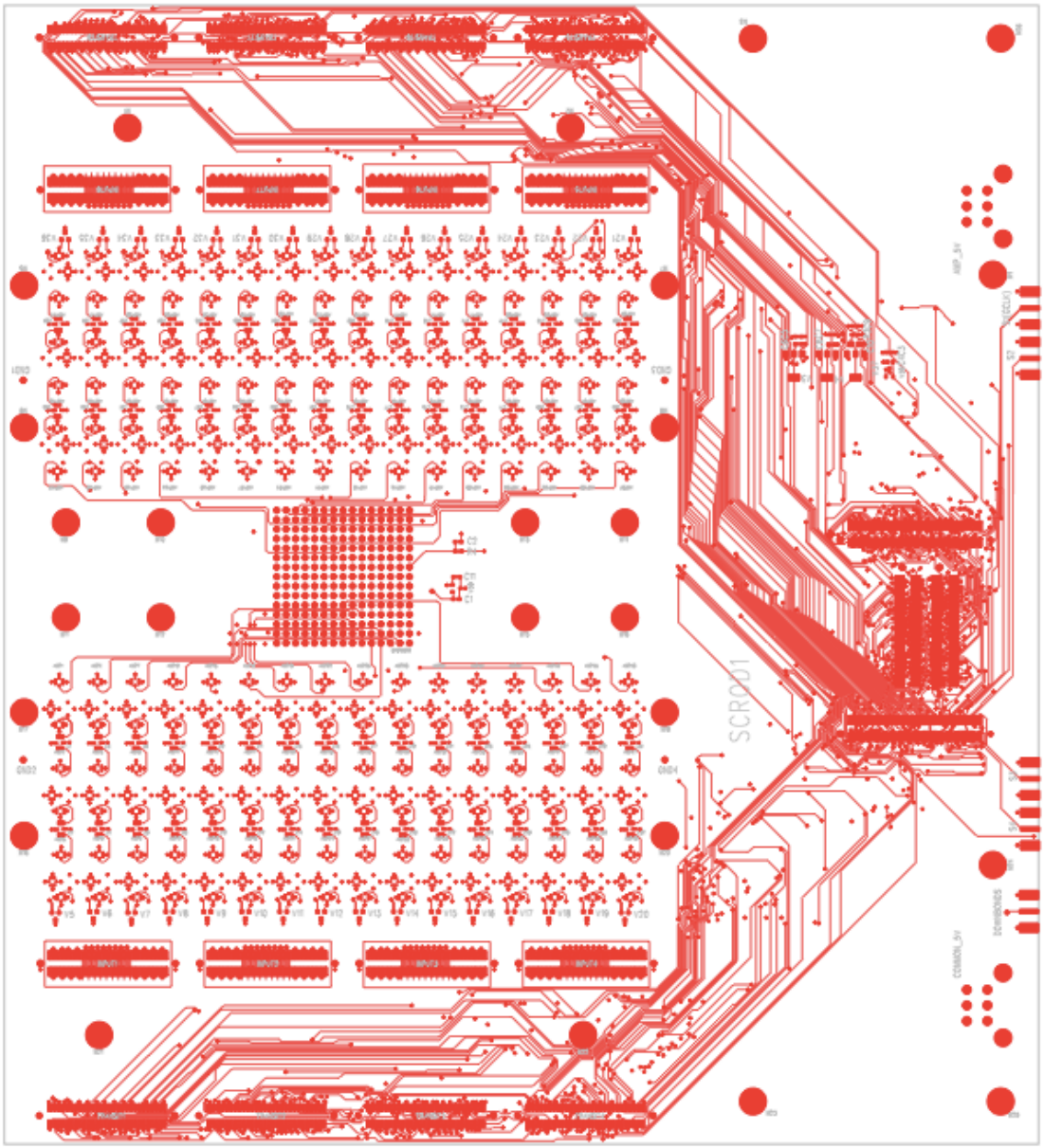
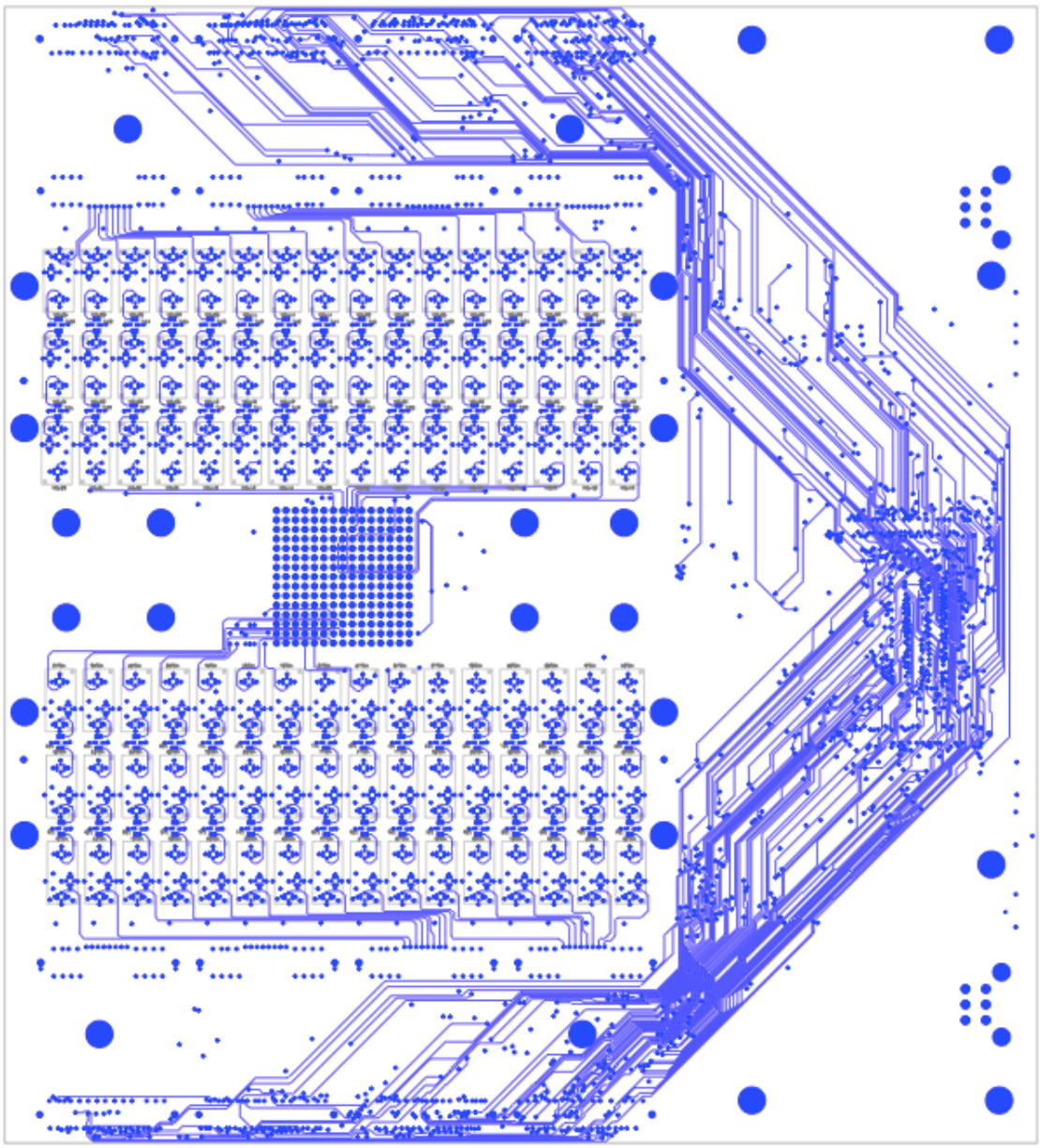


Motherboard top layer



Motherboard bottom layer

STURM2 Motherboard

Layer Definitions

Top Layer no plane routing / components

Layer 2 mixed plane split VPED / downbonds / routing

Layer 3 mixed plane amplifier regulator power

Layer 4 mixed plane amplifier power / routing

Layer 5 mixed plane ground plane 1 / routing

Layer 6 mixed plane common 5 volt power

Layer 7 mixed plane ground plane 2

Bottom Layer no plane routing / components

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
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revision:	B
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH, JH
PCB design:	JM, MZA, GSV, JH
sheet #:	1 of 17
sheet description:	TOP Block
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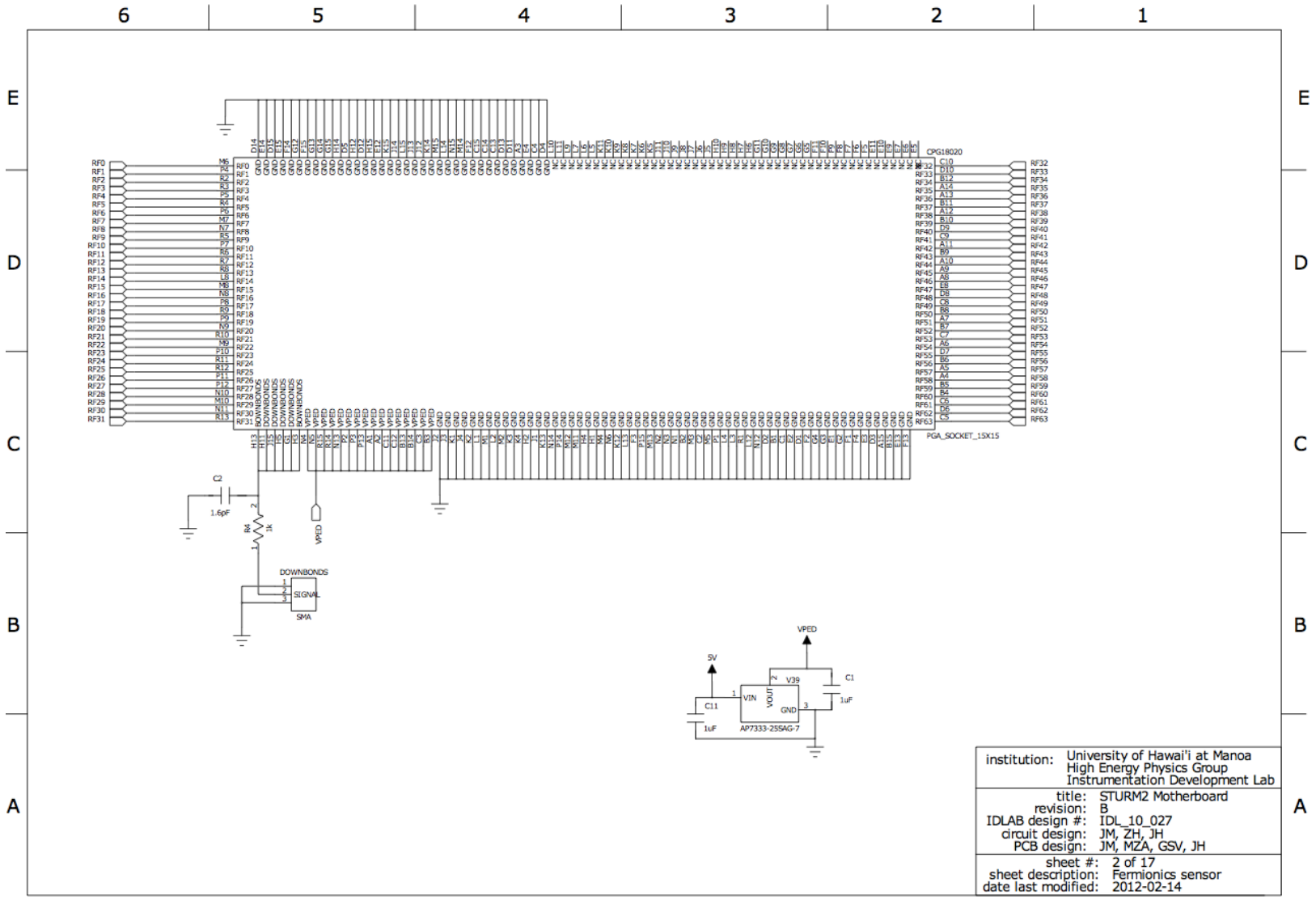
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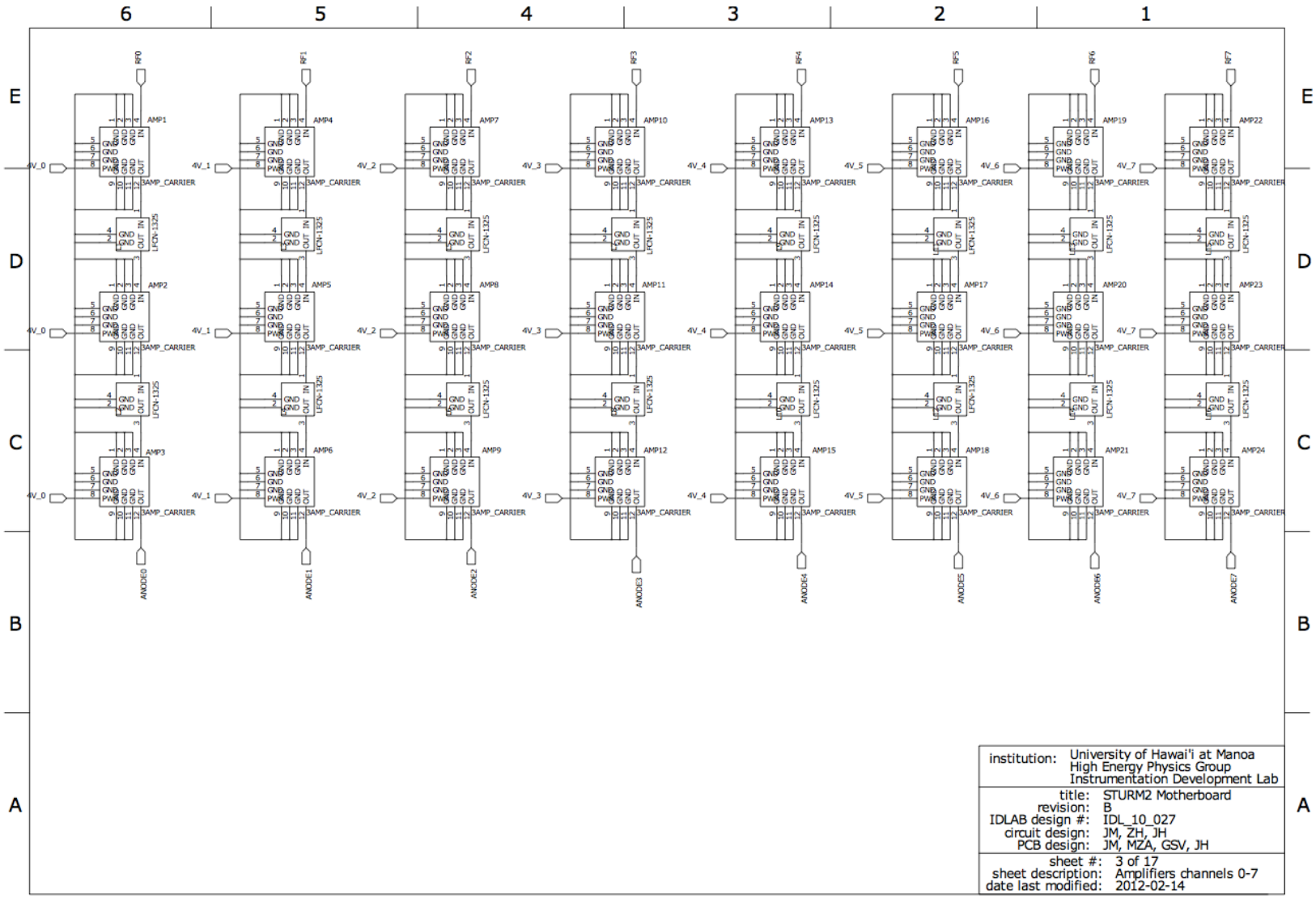
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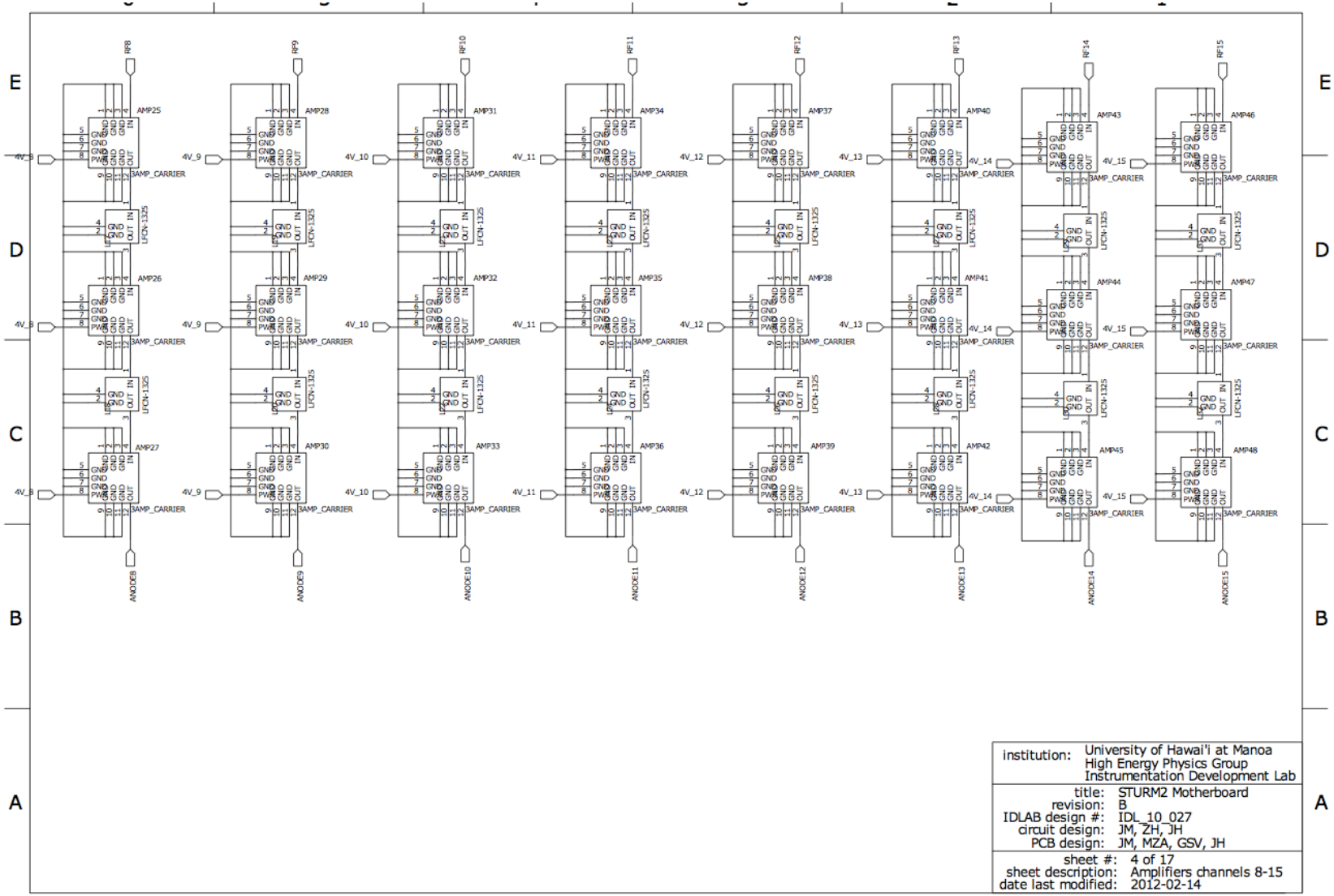
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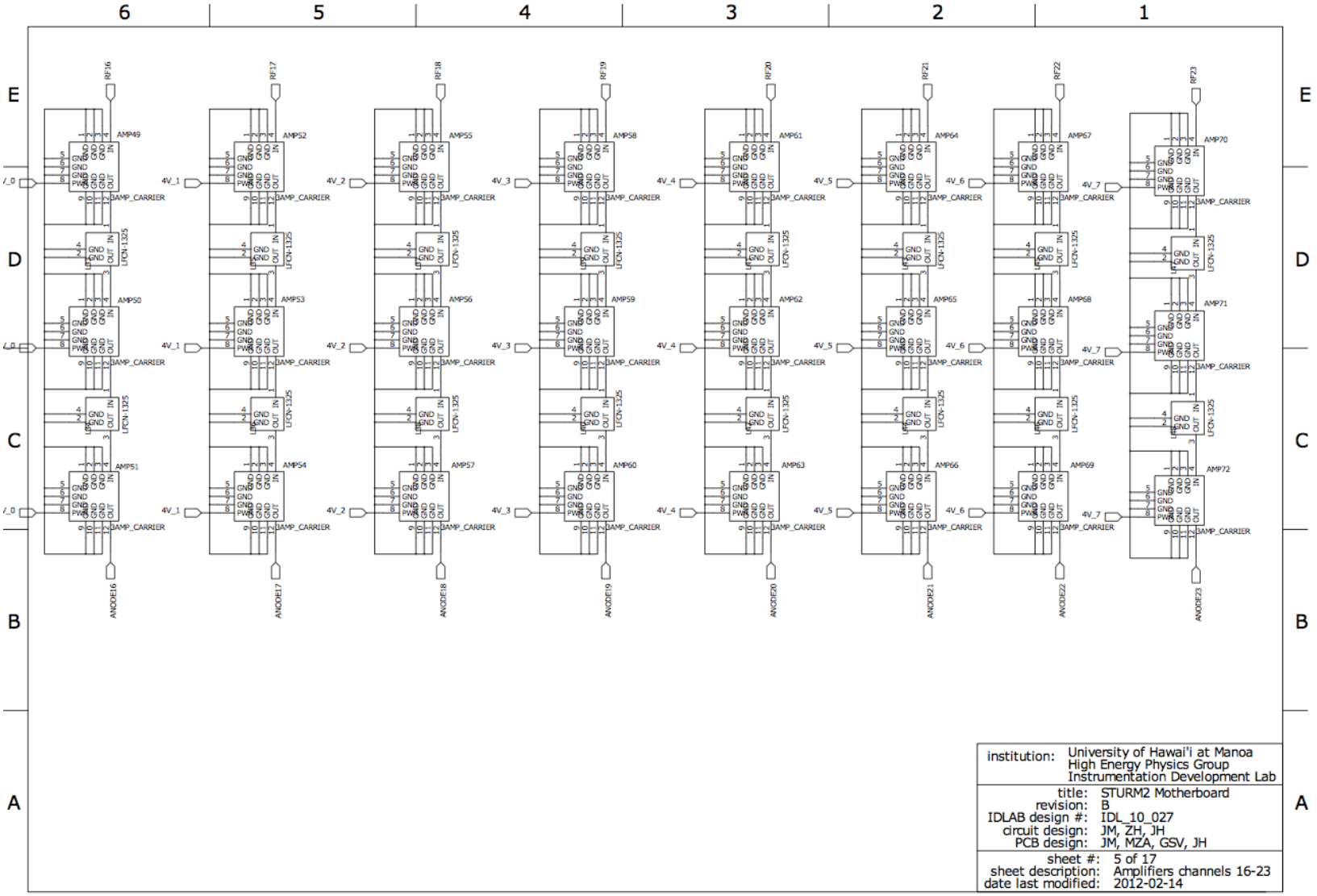
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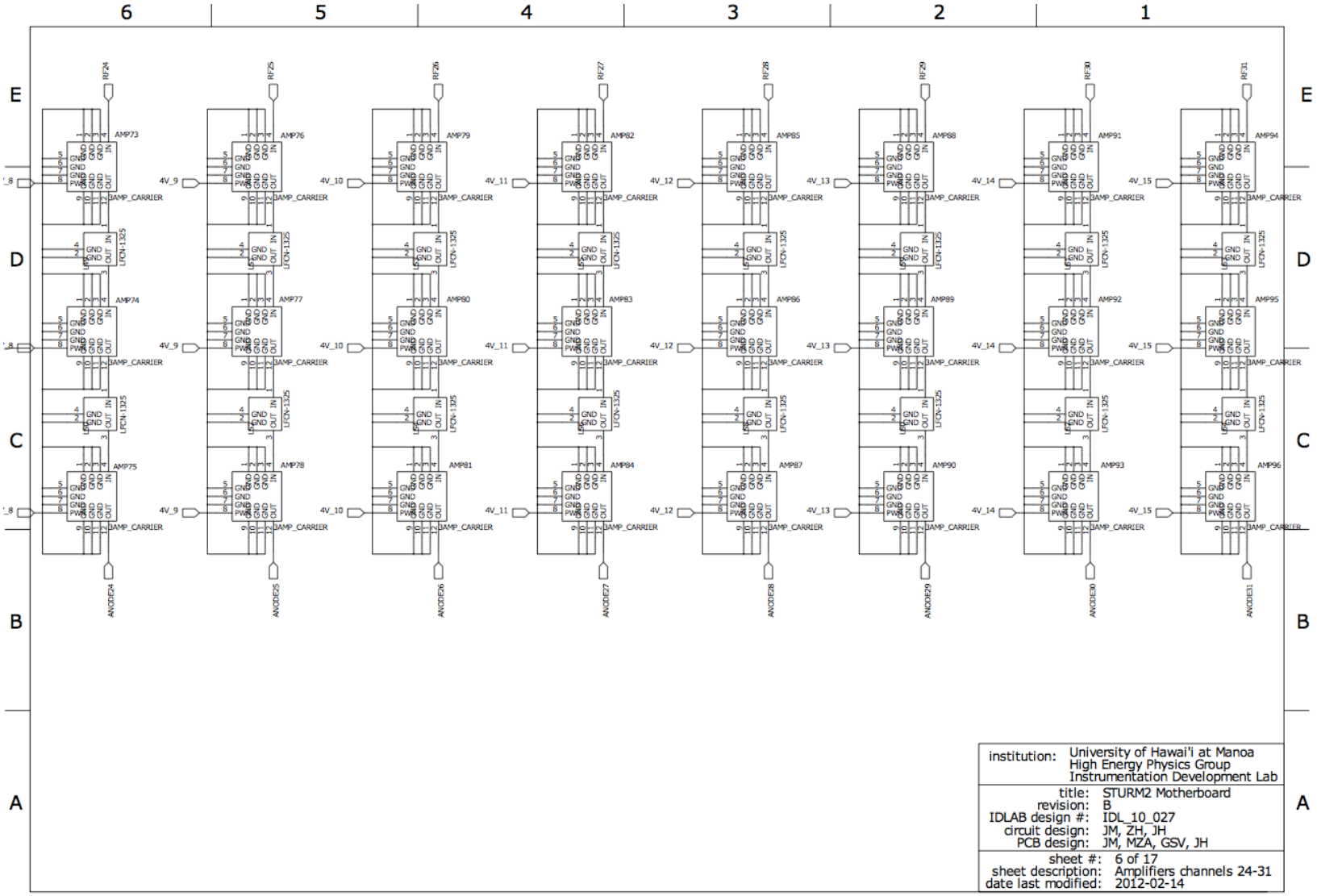
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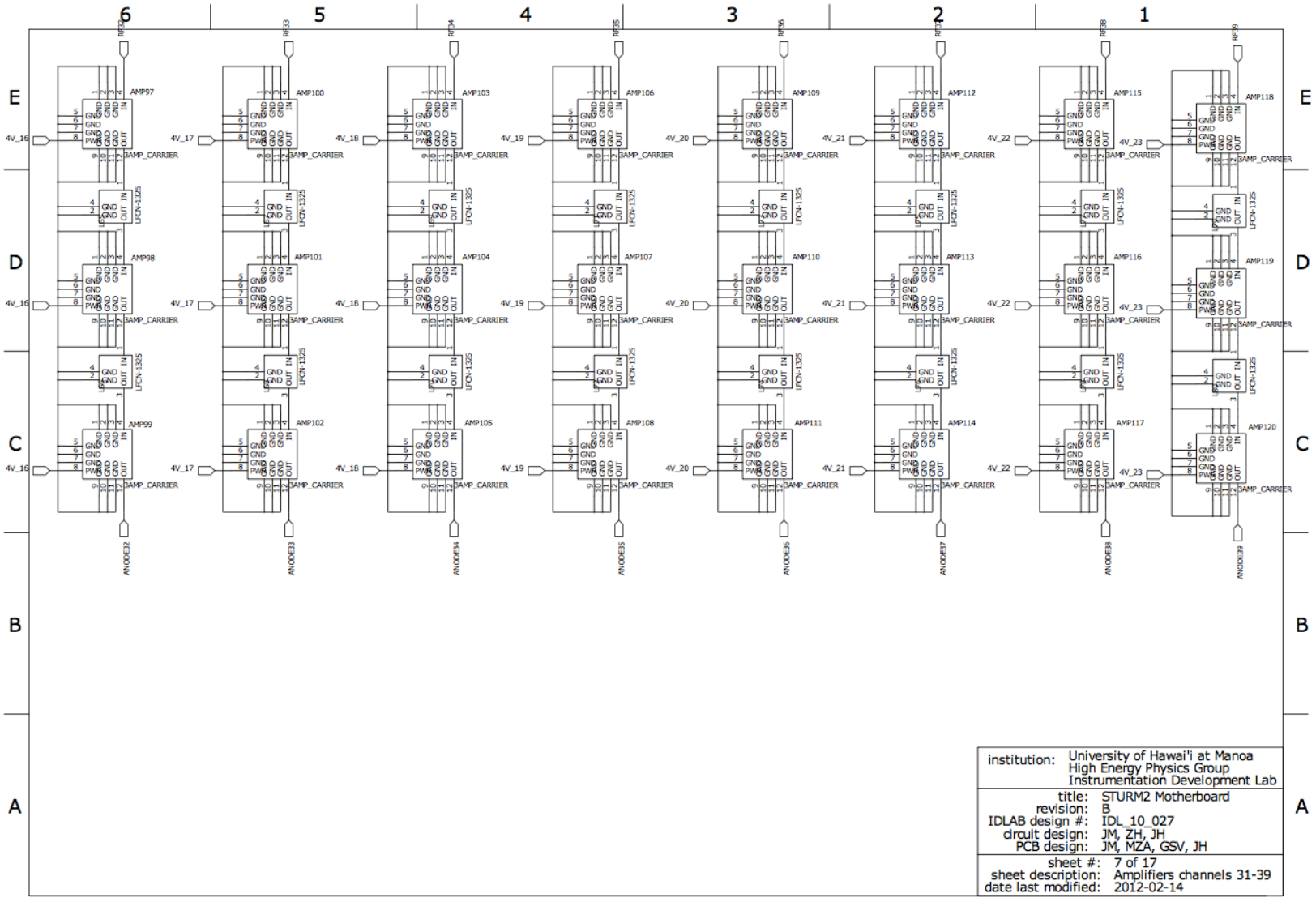
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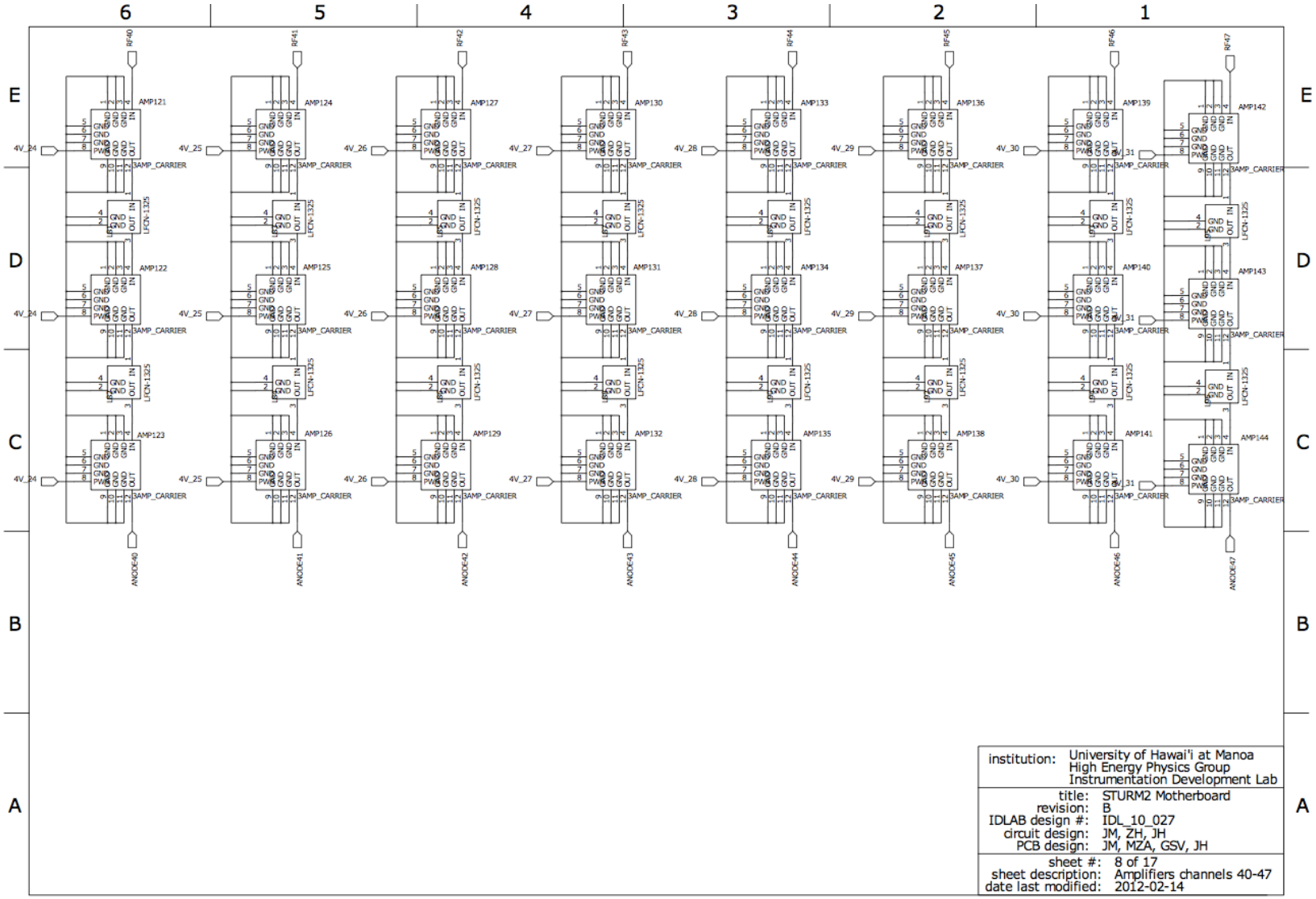
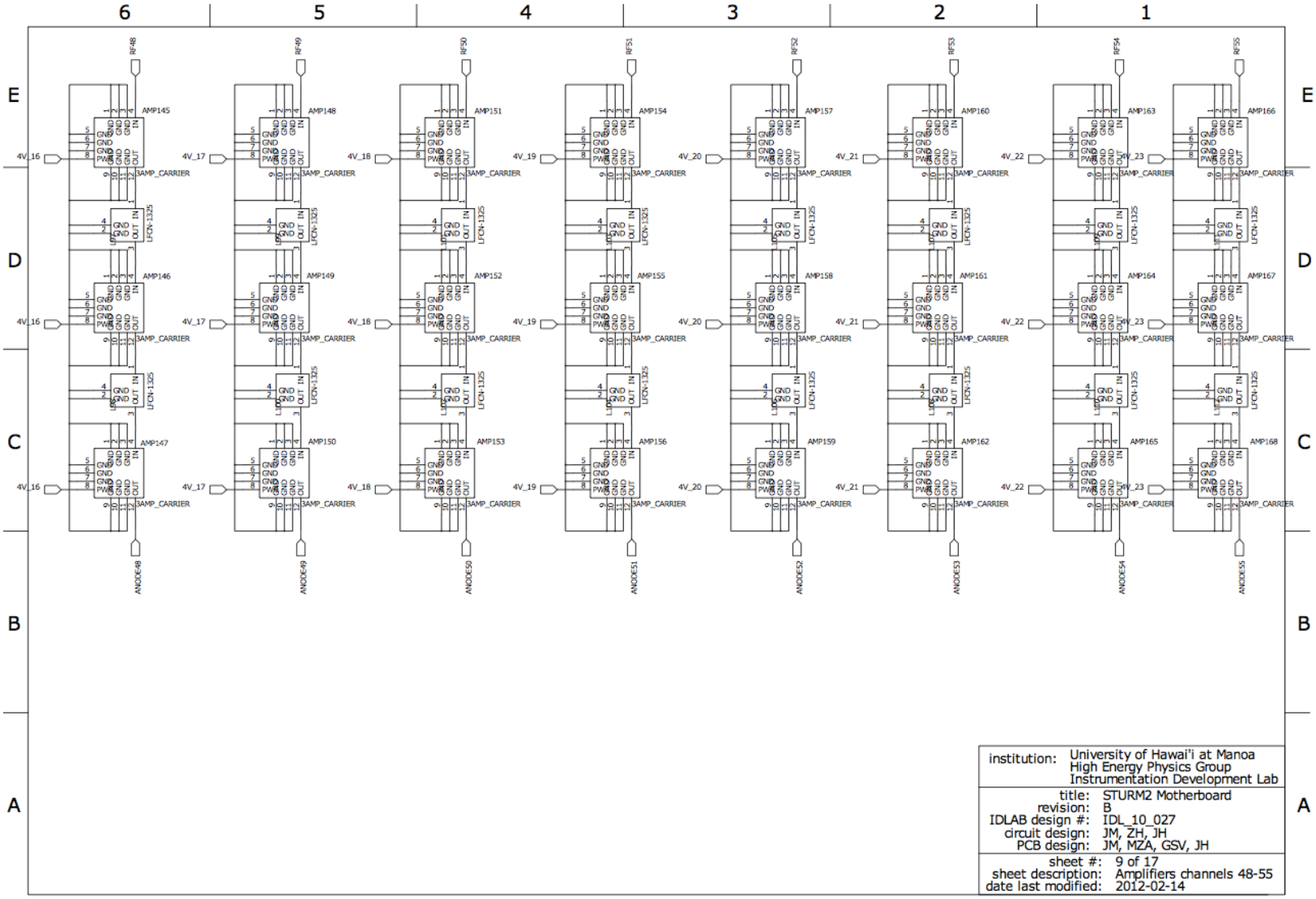
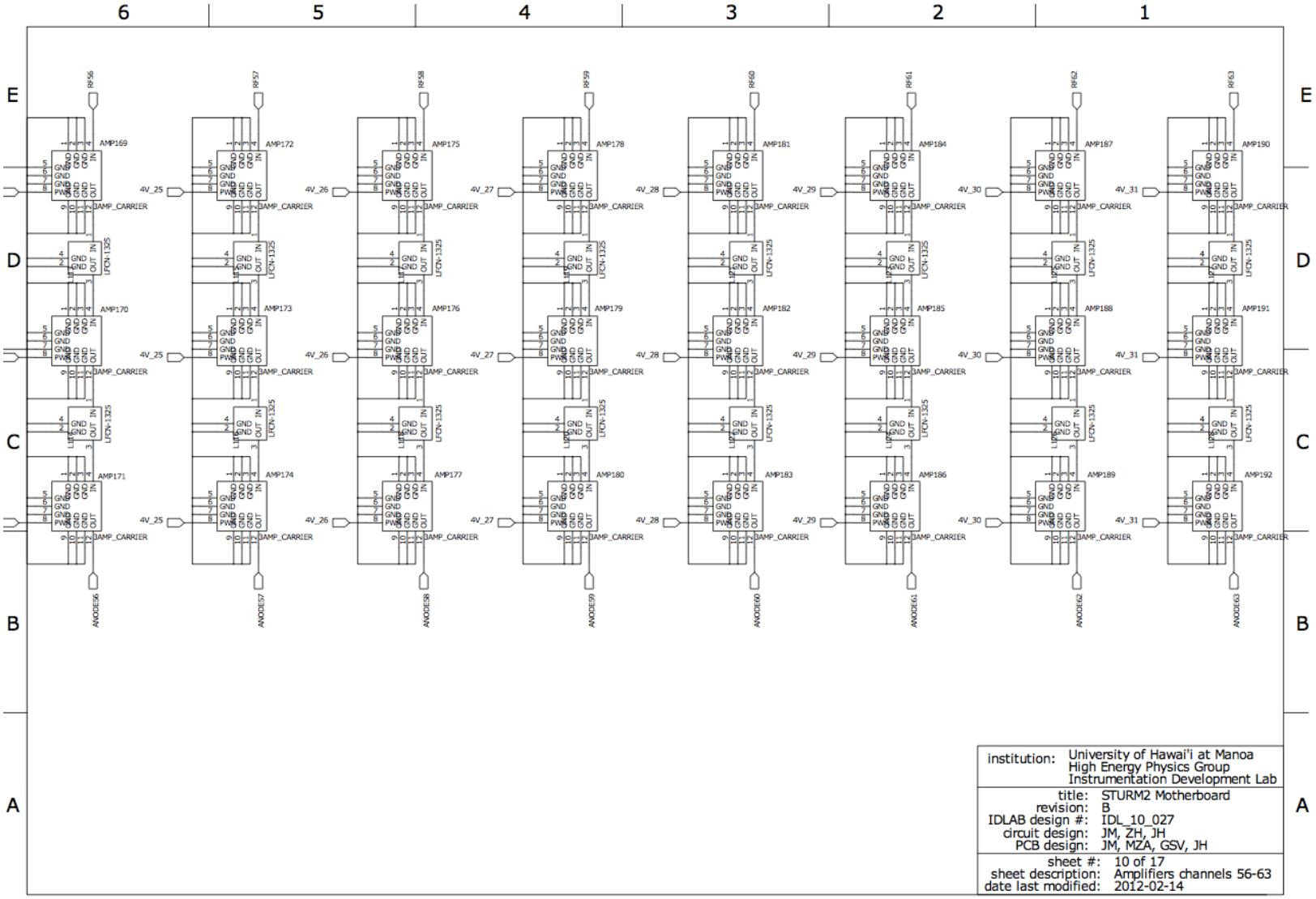
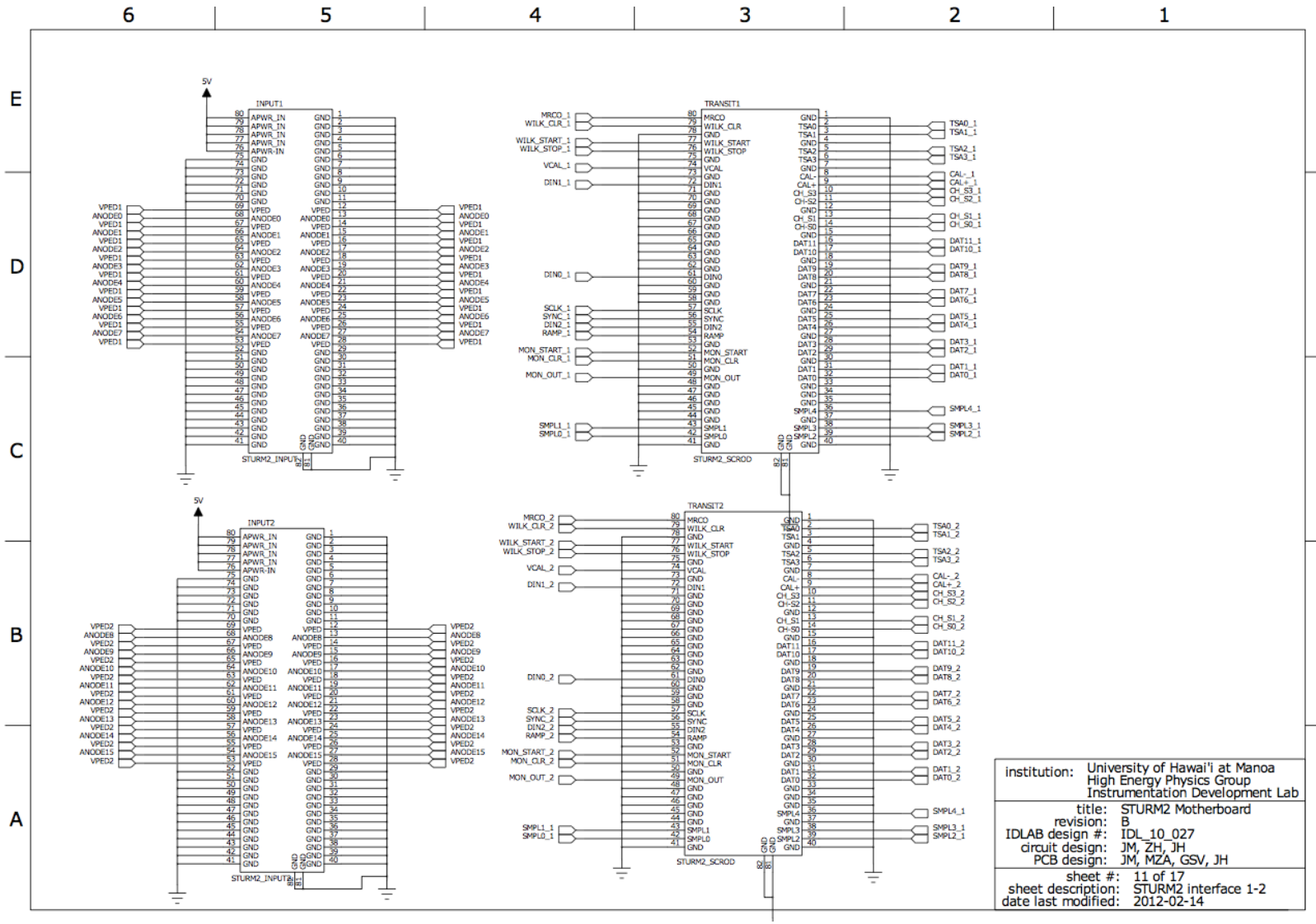
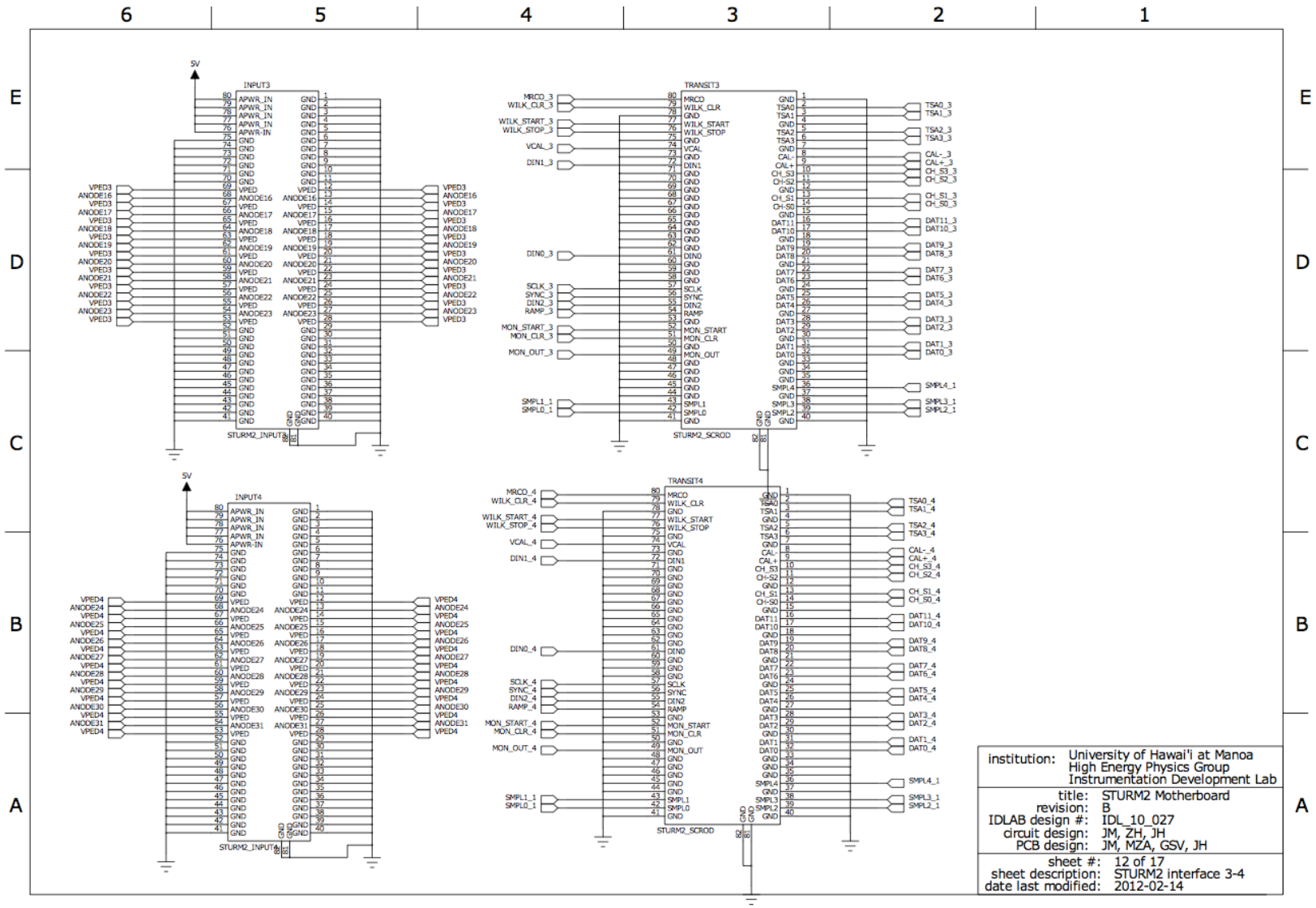
sheet description: Amplifiers channels 31-39
date last modified: 2012-02-14

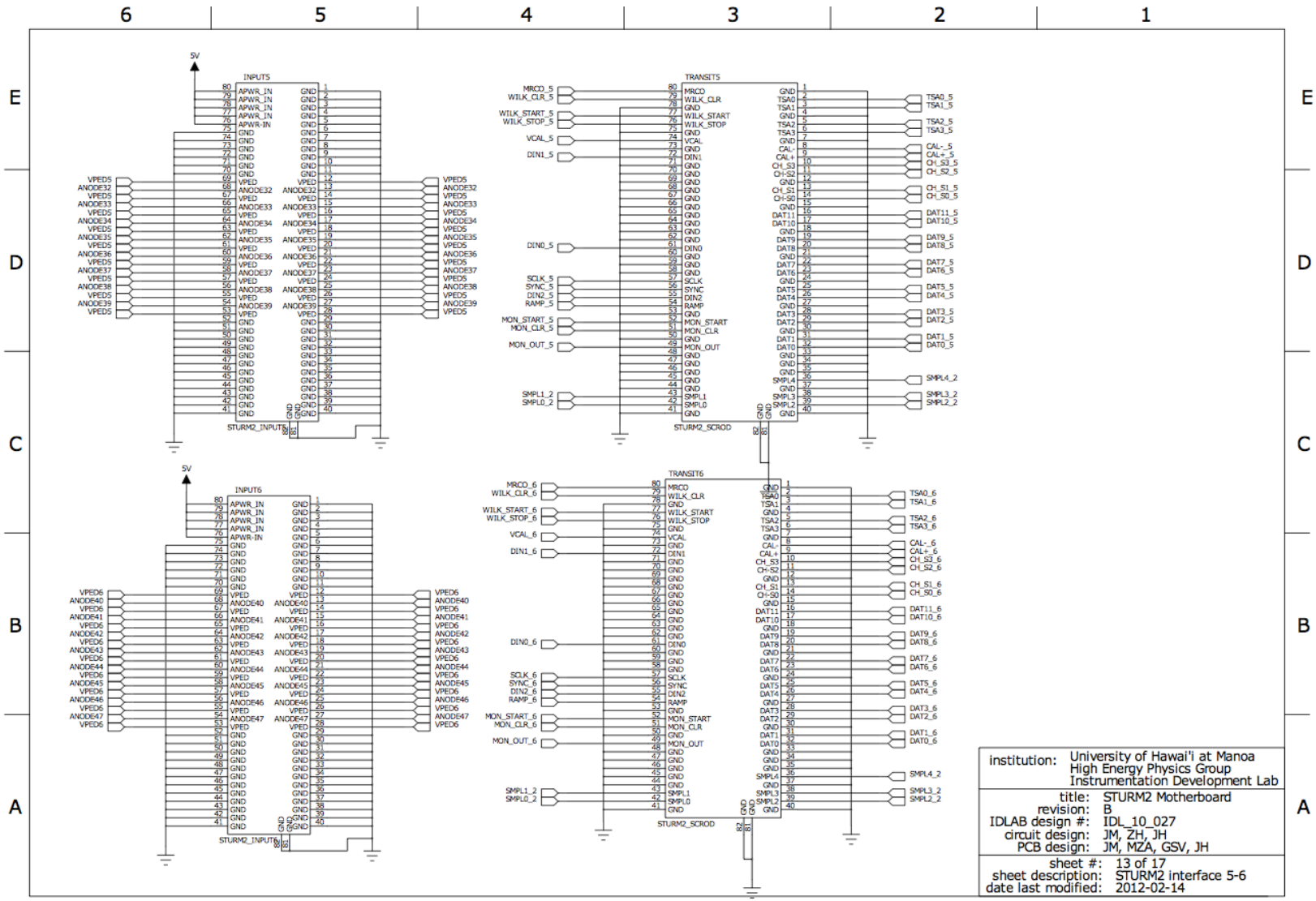

6
5
4
3
2
1
E
D
C
B
A
RF40
RF41
RF42
RF43
RF44
RF45
RF46
RF47
AMP121
AMP122
AMP123
AMP124
AMP125
AMP126
AMP127
AMP128
AMP129
AMP130
AMP131
AMP132
AMP133
AMP134
AMP135
AMP136
AMP137
AMP138
AMP139
AMP140
AMP141
AMP142
AMP143
AMP144
3AMP_CARRIER
LFCN-1325
4V_24
4V_25
4V_26
4V_27
4V_28
4V_29
4V_30
4V_31
ANODE40
ANODE41
ANODE42
ANODE43
ANODE44
ANODE45
ANODE46
ANODE47
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 8 of 17
sheet description: Amplifiers channels 40-47
date last modified: 2012-02-14

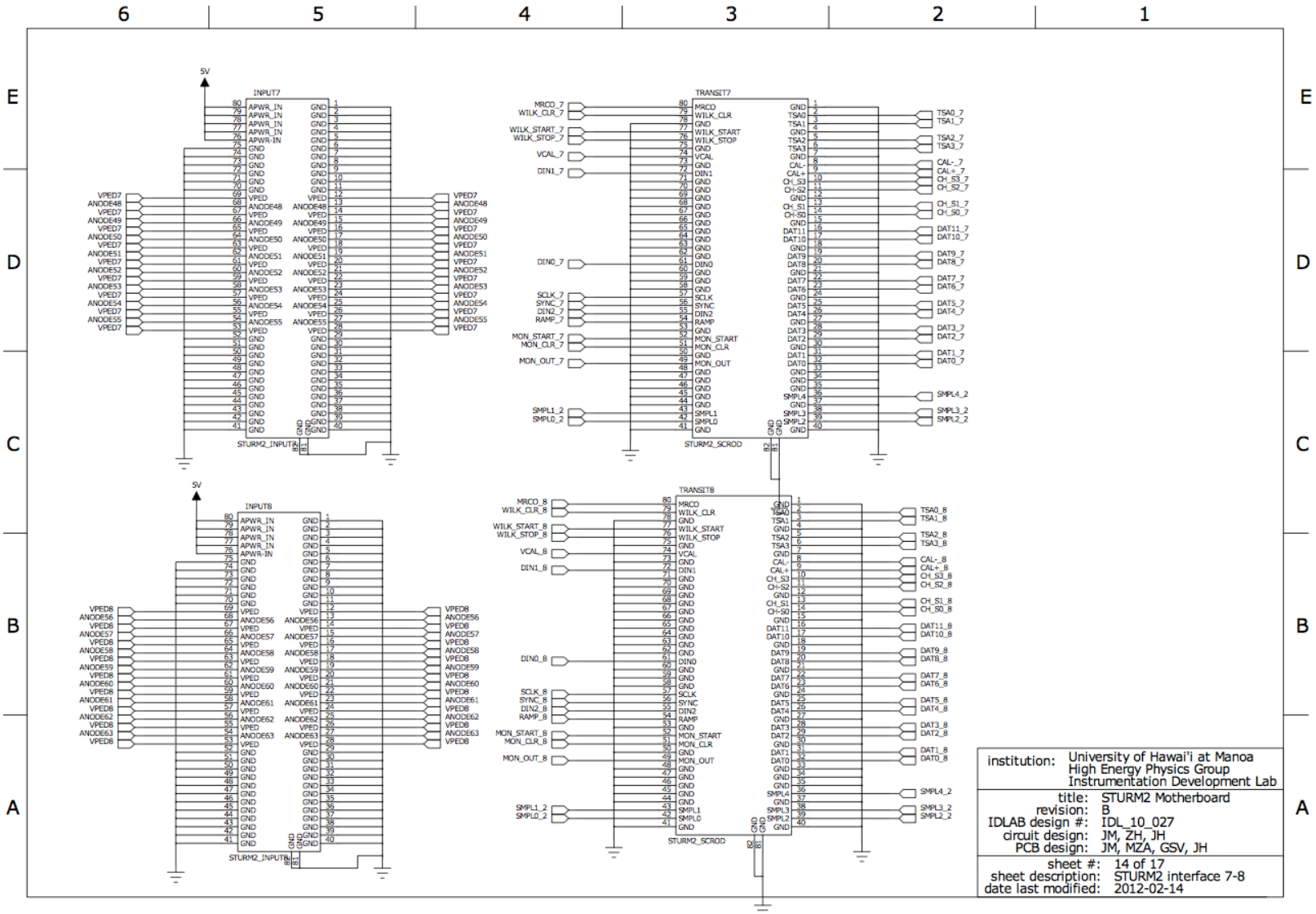

6
5
4
3
2
1
E
D
C
B
A
RF48
RF49
RF50
RF51
RF52
RF53
RF54
RF55
AMP145
AMP146
AMP147
AMP148
AMP149
AMP150
AMP151
AMP152
AMP153
AMP154
AMP155
AMP156
AMP157
AMP158
AMP159
AMP160
AMP161
AMP162
AMP163
AMP164
AMP165
AMP166
AMP167
AMP168
3AMP_CARRIER
LFCN-1325
LFCN-1320
4V_16
4V_17
4V_18
4V_19
4V_20
4V_21
4V_22
4V_23
ANODE48
ANODE49
ANODE50
ANODE51
ANODE52
ANODE53
ANODE54
ANODE55
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 9 of 17
sheet description: Amplifiers channels 48-55
date last modified: 2012-02-14

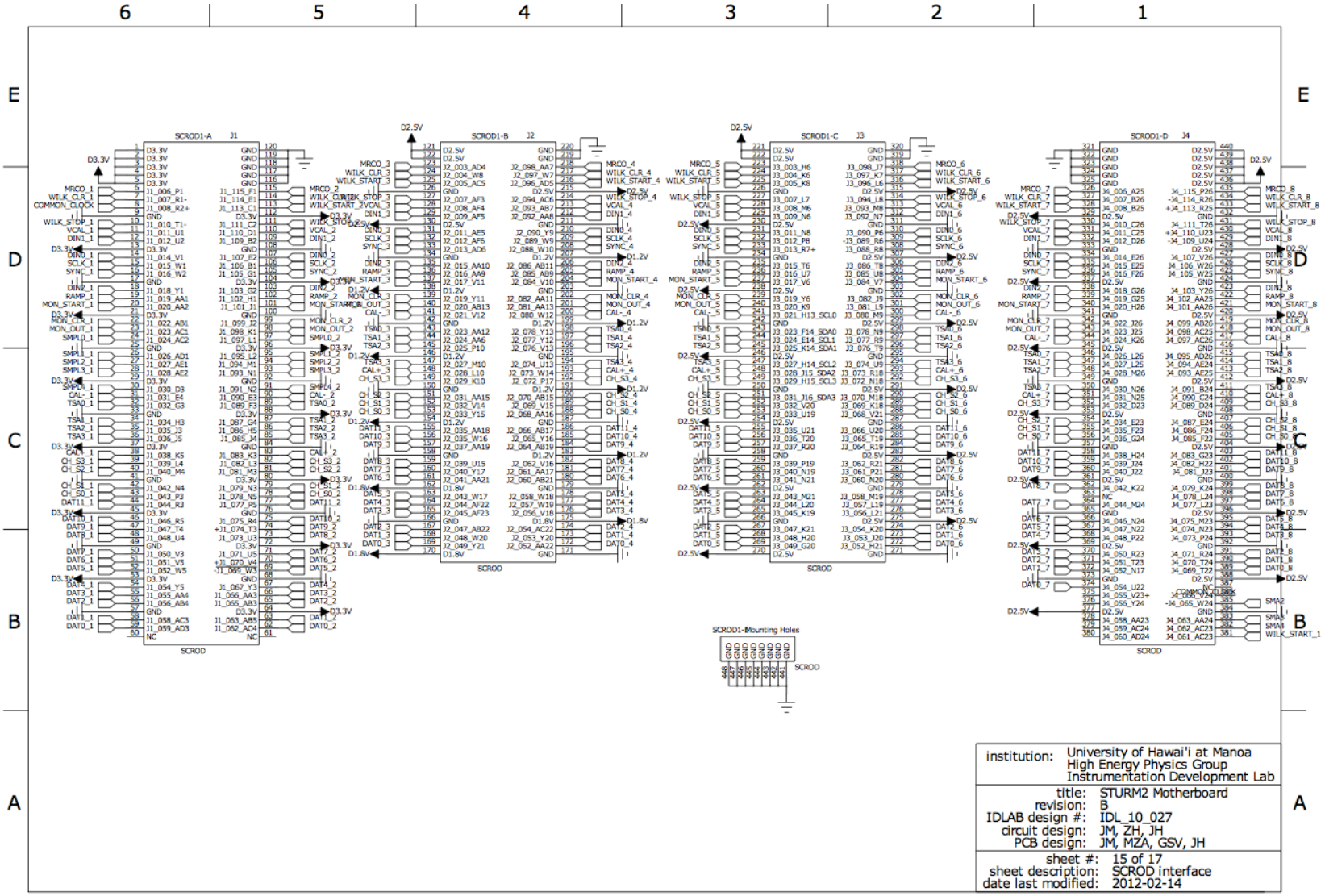

6
5
4
3
2
1
E
D
C
B
A
RP56
RP57
RP58
RP59
RP60
RP61
RP62
RP63
AMP169
AMP172
AMP175
AMP178
AMP181
AMP184
AMP187
AMP190
AMP170
AMP173
AMP176
AMP179
AMP182
AMP185
AMP188
AMP191
AMP171
AMP174
AMP177
AMP180
AMP183
AMP186
AMP189
AMP192
4V_25
4V_26
4V_27
4V_28
4V_29
4V_30
4V_31
3AMP_CARRIER
LFCN-1325
ANODE56
ANODE57
ANODE58
ANODE59
ANODE60
ANODE61
ANODE62
ANODE63
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 10 of 17
sheet description: Amplifiers channels 56-63
date last modified: 2012-02-14

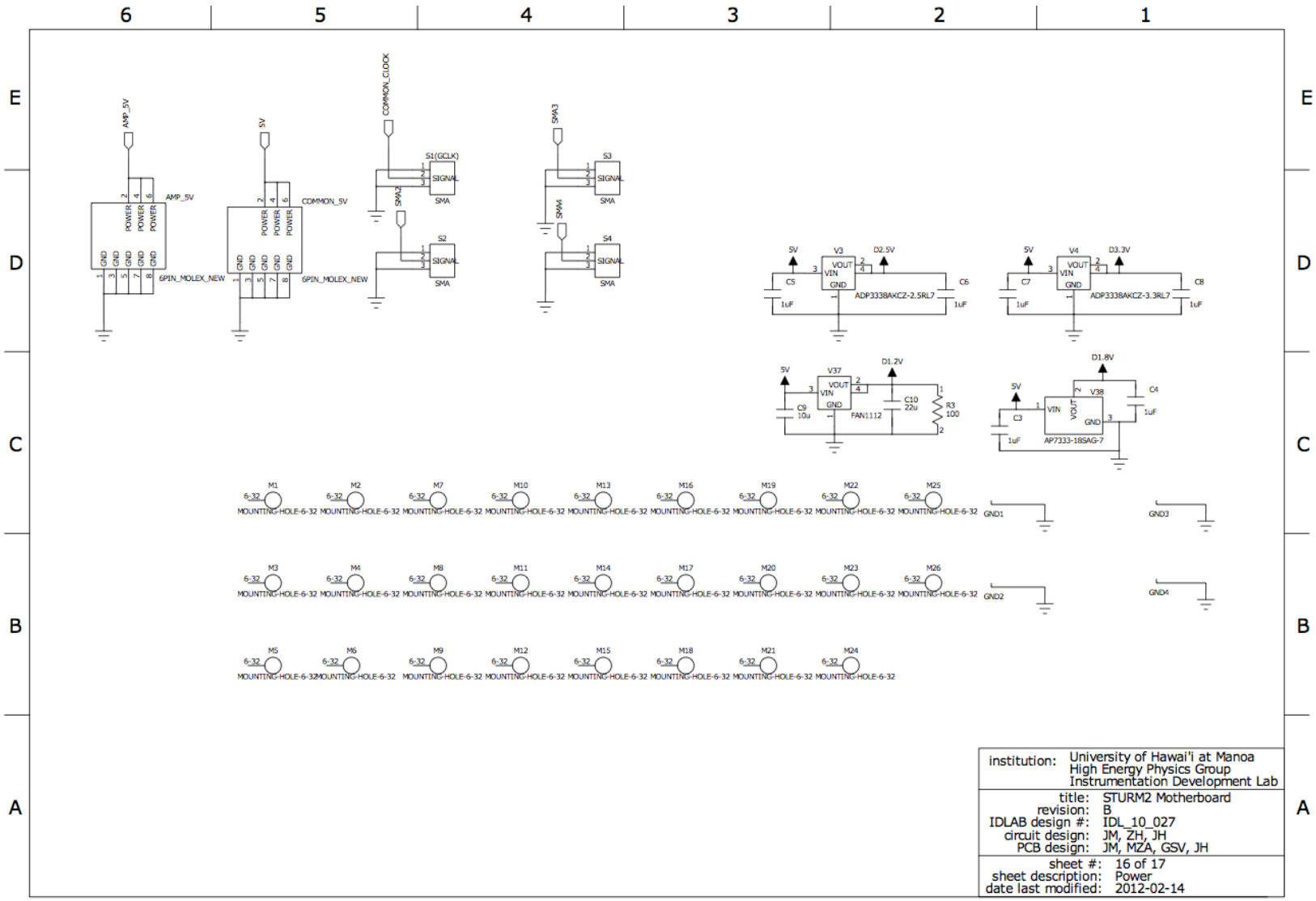

6
5
4
3
2
1
E
D
C
B
A
5V
INPUT1
STURM2_INPUT
TRANSIT1
STURM2_SCROD
INPUT2
STURM2_INPUT
TRANSIT2
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 11 of 17
sheet description: STURM2 interface 1-2
date last modified: 2012-02-14

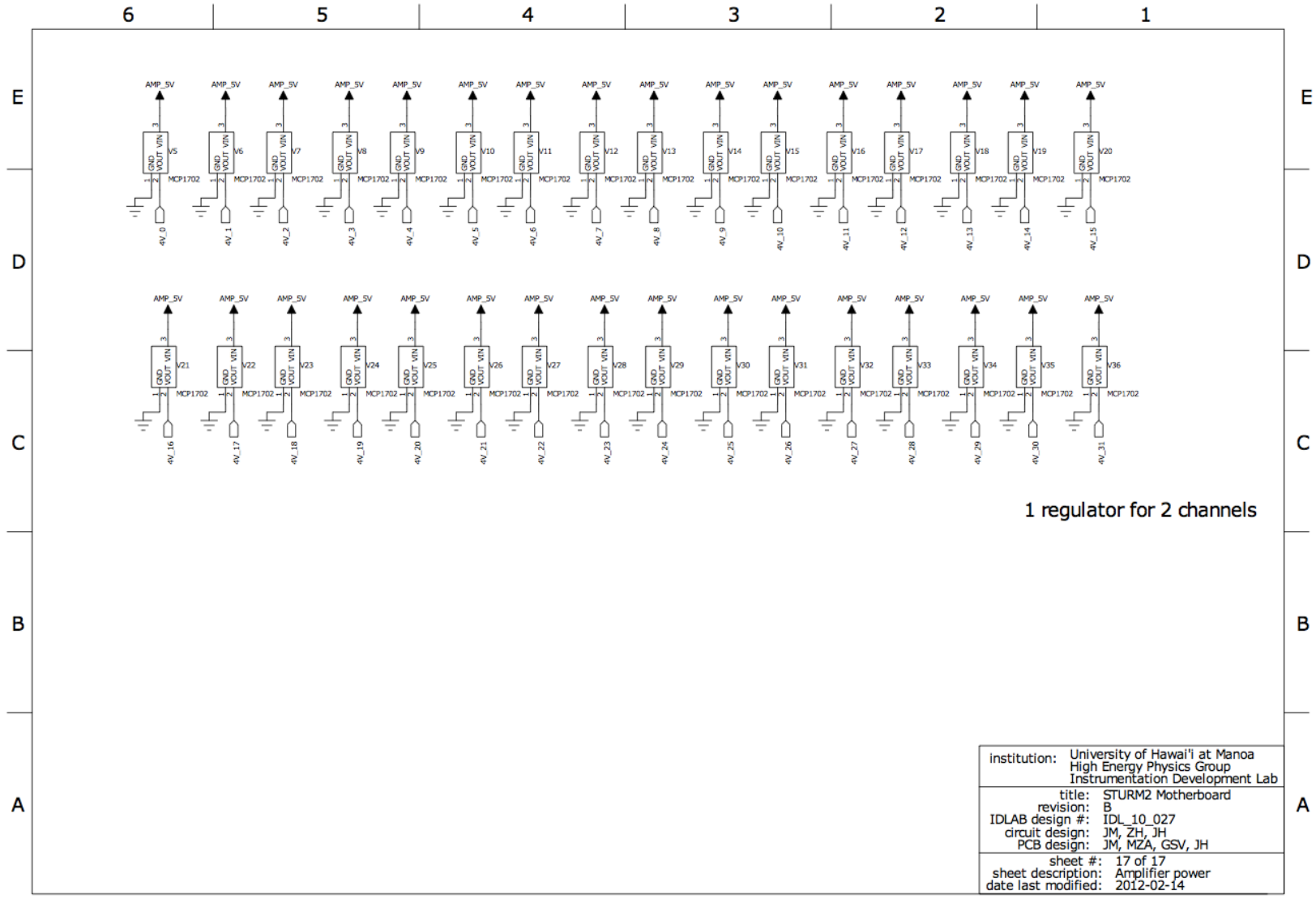

6
5
4
3
2
1
E
D
C
B
A
5V
INPUT3
STURM2_INPUT3
TRANSIT3
STURM2_SCROD
INPUT4
STURM2_INPUT4
TRANSIT4
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 12 of 17
sheet description: STURM2 interface 3-4
date last modified: 2012-02-14


6
5
4
3
2
1
E
D
C
B
A
5V
INPUT5
STURM2_INPUT5
TRANSIT5
STURM2_SCROD
INPUT6
STURM2_INPUT6
TRANSIT6
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 13 of 17
sheet description: STURM2 interface 5-6
date last modified: 2012-02-14


6
5
4
3
2
1
E
D
C
B
A
INPUT7
STURM2_INPUT7
INPUT8
STURM2_INPUT8
TRANSIT7
STURM2_SCROD
TRANSIT8
STURM2_SCROD
5V
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 14 of 17
sheet description: STURM2 interface 7-8
date last modified: 2012-02-14


6
5
4
3
2
1
E
D
C
B
A
SCROD1-A J1
SCROD1-B J2
SCROD1-C J3
SCROD1-D J4
SCROD
SCROD1-Mounting Holes
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 15 of 17
sheet description: SCROD interface
date last modified: 2012-02-14


6
5
4
3
2
1
E
D
C
B
A
AMP_5V
5V
COMMON_CLOCK
SMA3
S1(GCLK)
S2
S3
S4
SIGNAL
SMA
SMA2
SMA4
POWER
GND
AMP_5V
COMMON_5V
6PIN_MOLEX_NEW
V3
V4
V37
V38
VOUT
VIN
GND
D2.5V
D3.3V
D1.2V
D1.8V
C5
C6
C7
C8
C9
C10
C3
C4
R3
1uF
10u
22u
100
ADP3338AKCZ-2.5RL7
ADP3338AKCZ-3.3RL7
FAN1112
AP7333-18SAG-7
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
6-32
MOUNTING-HOLE-6-32
GND1
GND2
GND3
GND4
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 16 of 17
sheet description: Power
date last modified: 2012-02-14


6
5
4
3
2
1
E
D
C
B
A
AMP_5V
GND
VOUT
VIN
MCP1702
4V_0
4V_1
4V_2
4V_3
4V_4
4V_5
4V_6
4V_7
4V_8
4V_9
4V_10
4V_11
4V_12
4V_13
4V_14
4V_15
4V_16
4V_17
4V_18
4V_19
4V_20
4V_21
4V_22
4V_23
4V_24
4V_25
4V_26
4V_27
4V_28
4V_29
4V_30
4V_31
1 regulator for 2 channels
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: B
IDLAB design #: IDL_10_027
circuit design: JM, ZH, JH
PCB design: JM, MZA, GSV, JH
sheet #: 17 of 17
sheet description: Amplifier power
date last modified: 2012-02-14

```
NET BCLKp       LOC = "U25"     | IOSTANDARD = LVDS_25;# | diff_term = true;       #CLK_MAIN to BCLK
NET BCLKn       LOC = "U26"     | IOSTANDARD = LVDS_25;# | diff_term = true;       #CLK_MAIN to BCLK

##########################################################################
## STURM2 ASIC I/Os
##########################################################################
NET RAMP        LOC = "AA1"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TST_START LOC = "AA2"       | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TST_CLR     LOC = "AB1"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TST_OUT     LOC = "AC1"     | IOSTANDARD = LVCMOS25;
NET SMPL_SEL<0>                 LOC = "AC2"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET SMPL_SEL<1>                 LOC = "AD1"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET SMPL_SEL<2>                 LOC = "AE1"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET SMPL_SEL<3>                 LOC = "AE2"     | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET SMPL_SEL<4>                 LOC = "D3"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET DAT<0>      LOC = "AD3"     | IOSTANDARD = LVCMOS25;
NET DAT<1>      LOC = "AC3"     | IOSTANDARD = LVCMOS25;
NET DAT<2>      LOC = "AB4"     | IOSTANDARD = LVCMOS25;
NET DAT<3>      LOC = "AA4"     | IOSTANDARD = LVCMOS25;
NET DAT<4>      LOC = "Y5"      | IOSTANDARD = LVCMOS25;
NET DAT<5>      LOC = "W5"      | IOSTANDARD = LVCMOS25;
NET DAT<6>      LOC = "V5"      | IOSTANDARD = LVCMOS25;
NET DAT<7>      LOC = "V3"      | IOSTANDARD = LVCMOS25;
NET DAT<8>      LOC = "U4"      | IOSTANDARD = LVCMOS25;
NET DAT<9>      LOC = "T4"      | IOSTANDARD = LVCMOS25;
NET DAT<10>     LOC = "R5"      | IOSTANDARD = LVCMOS25;
NET DAT<11>     LOC = "R3"      | IOSTANDARD = LVCMOS25;
NET CH_SEL<0> LOC = "P3"        | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET CH_SEL<1> LOC = "N4"        | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET CH_SEL<2> LOC = "M4"        | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET CH_SEL<3> LOC = "L4"        | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TDC_STOP  LOC = "T1"        | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TDC_START                   LOC = "AC23"    | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TDC_CLR     LOC = "R1"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET MRCO        LOC = "P1"      | IOSTANDARD = LVCMOS25;
NET TSA_OUT<0>                  LOC = "G3"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TSA_OUT<1>                  LOC = "H3"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TSA_OUT<2>                  LOC = "J3"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET TSA_OUT<3>                  LOC = "J5"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
##########################################################################
## USB I/O
##########################################################################
NET IFCLK       LOC = "B14"     | IOSTANDARD = LVCMOS33;# |  CLOCK_DEDICATED_ROUTE = FALSE;
NET CLKOUT      LOC = "E13"     | IOSTANDARD = LVCMOS33; #  "E13"
ET PA0          LOC = "G7"      | IOSTANDARD = LVCMOS33;
NET PA1         LOC = "H8"      | IOSTANDARD = LVCMOS33;
NET PA2         LOC = "G8"      | IOSTANDARD = LVCMOS33;
NET PA3         LOC = "F7"      | IOSTANDARD = LVCMOS33;
NET PA4         LOC = "F6"      | IOSTANDARD = LVCMOS33;
NET PA5         LOC = "C3"      | IOSTANDARD = LVCMOS33;
NET PA6         LOC = "B3"      | IOSTANDARD = LVCMOS33;
NET PA7         LOC = "G6"      | IOSTANDARD = LVCMOS33;
```

```
NET FD<0>       LOC = "F5"       | IOSTANDARD = LVCMOS33;
NET FD<1>       LOC = "E6"       | IOSTANDARD = LVCMOS33;
NET FD<2>       LOC = "E5"       | IOSTANDARD = LVCMOS33;
NET FD<3>       LOC = "H9"       | IOSTANDARD = LVCMOS33;
NET FD<4>       LOC = "G9"       | IOSTANDARD = LVCMOS33;
NET FD<5>       LOC = "A3"       | IOSTANDARD = LVCMOS33;
NET FD<6>       LOC = "A2"       | IOSTANDARD = LVCMOS33;
NET FD<7>       LOC = "F9"       | IOSTANDARD = LVCMOS33;
NET FD<8>       LOC = "E8"       | IOSTANDARD = LVCMOS33;
NET FD<9>       LOC = "D5"       | IOSTANDARD = LVCMOS33;
NET FD<10>      LOC = "C5"       | IOSTANDARD = LVCMOS33;
NET FD<11>      LOC = "H10"      | IOSTANDARD = LVCMOS33;
NET FD<12>      LOC = "G10"      | IOSTANDARD = LVCMOS33;
NET FD<13>      LOC = "B4"       | IOSTANDARD = LVCMOS33;
NET FD<14>      LOC = "A4"       | IOSTANDARD = LVCMOS33;
NET FD<15>      LOC = "F10"      | IOSTANDARD = LVCMOS33;
NET CTL0        LOC = "F12"      | IOSTANDARD = LVCMOS33;
NET CTL1        LOC = "E12"      | IOSTANDARD = LVCMOS33;
NET CTL2        LOC = "J11"      | IOSTANDARD = LVCMOS33;
NET RDY0        LOC = "G11"      | IOSTANDARD = LVCMOS33;
NET RDY1        LOC = "H12"      | IOSTANDARD = LVCMOS33;
NET WAKEUP      LOC = "F11"      | IOSTANDARD = LVCMOS33;
##########################################################################
## DAC I/O
##########################################################################
NET SCLK         LOC = "W1"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET SYNC         LOC = "W2"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET DIN0         LOC = "V1"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET DIN1         LOC = "U2"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
NET DIN2         LOC = "Y1"      | IOSTANDARD = LVCMOS25 | DRIVE = 12 | SLEW = FAST ;
##########################################################################
## User I/O
##########################################################################
NET LED_0       LOC = "F18"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;#GREEN
#NET LED_1      LOC = "E18"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_2      LOC = "G16"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_3      LOC = "F17"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_4      LOC = "F20"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_5      LOC = "E20"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_6      LOC = "H17"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
NET LED_7       LOC = "G17"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_8       LOC = "C21"     | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_9      LOC = "B21"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
NET LED_A       LOC = "H18"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
NET LED_B       LOC = "H19"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_C      LOC = "B22"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_D      LOC = "A22"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
#NET LED_E      LOC = "G19"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;
NET LED_F       LOC = "F19"      | IOSTANDARD = LVCMOS33 | DRIVE = 12 | SLEW = SLOW ;#RED
##########################################################################################
NET "xCLK" TNM_NET = TxCLK;
TIMESPEC TSxCLK = PERIOD "TxCLK" 10 ns HIGH 50% PRIORITY 1;
```

```
NET "xUSB_MAIN/USB_CLK" TNM_NET = TxIFCLK;
#NET "xIFCLK" TNM_NET = TxIFCLK;
TIMESPEC TSxIFCLK = PERIOD "TxIFCLK" 20 ns HIGH 50% PRIORITY 5;
```

Appendix 4

Varner, G. 2012. About my thesis and pictures [email]. Recipients: Ari Parviainen; Janne, Himanen; Jussi Kangaskoski; Lauri Karppinen; Vihtori Virta. Sent 30 May 2012 [accessed 30 May 2012].


SAVONIA